AUSTRALIAN RAIL TRACK CORPORATION LTD

Discipline: Engineering (Signalling) **Category: Procedure**

Microlok Data Design Records
(Addressing, File Control, Checking, and FAT Testing)

ESD-05-11

Applicability

ARTC Network Wide	✓

Primary Source

Signal Engineering Technical Notes: EST-06-03A Microlok Data Control & Testing, EST-06-04A Retesting Microlok Data & EST-06-05A Checking Microlok Data Designs.

Document Status

Version	Date Reviewed	Prepared by	Reviewed by	Endorsed	Approved
1.3	17 Feb 14	Standards	Stakeholders	Manager Standards	General Manager Technical Standards 18/02/2014

Amendment Record

Version	Date Reviewed	Clause	Description of Amendment
1.0	24 Apr 09		First issue
1.1	07 Oct 09		Disclaimer updated as per Risk & Safety Committee 14/09/2009
1.2	13 Aug 10	All	Issued as final.
1.3	17 Feb 14	Appendix A	Updated example form.

Contents

1 Introduction

1.1 Purpose

The purpose of this Procedure is to describe the process management involved with the production of Microlok data. This includes the checking process during the review and verification of Microlok Data and the processes involved for the re-testing of Microlok data following a data change after the initial Design Integrity Test has been completed. The Procedure also provides guidelines on the Control of Microlok Data produced for Microlok applications.

1.2 Procedure Owner

The Manager Standards is the Procedure Owner and is the initial point of contact for all queries relating to this procedure.

1.3 Reference Documents

ARTC Documents

- Form ESD0511F-01 Request for Microlok II Address
- Form ESD0511F-02 Installed Microlok Data Form
- ESD-05-12 Design of Microlok II Interlockings
- ESD-25-02 Signal Engineering Design Management (Draft)
- ESD2503F-04 As-Designed Checklist (Draft)
- ESD2503F-05 As-Commission Checklist (Draft)
- ESD2503F-06 As-built Checklist (Draft)

1.4 Introduction

The Microlok II development system tools are to be used to develop and compile an application logic program, debug the program, and upload the application program to the Microlok II central processing unit (CPU) card.

For the comprehensive procedures to create the complete Microlok II application program, reference should be made to the US&S Microlok II System Application Logic Programming Guide, SM-6800D manual and Application Guidelines SM-6800G.

Design Engineers are to ensure the application logic is produced utilising the current approved Microlok II development tools and compilation software. Refer to current Type Approval for approved software versions.

The current approved versions of the Executive software shall also be used as detailed in the Type Approval. The Design and Verification processes shall ensure that these versions have been identified, documented and verified.

The application logic is to be designed in accordance with ESD-05-12 Design of Microlok II Interlockings.

2 Management of Microlok Data

2.1 Microlok Addresses

To obtain the Microlok Card File Address a "Request for Microlok II Address Form" (see Form *ESD0511F-01*) shall be completed, signed and sent to ARTC. The Signal Manager or nominated Signalling representative upon request may provide the Microlok II Card File Address. Only the supplied Card File Address shall be use for the programming.

2.2 Submission of As-Designed Microlok Data

The As-Designed Microlok Data does not need to be submitted with the As-Designed Documentation unless the contract is for Design only. However the Microlok Data Verification Report shall be submitted. The report shall be submitted along with all other As-Designed documentation as per ESD2503F-04 As-Designed Checklist.

This shall be submitted on CDRom. Separate CDRoms shall be provided for the Maintenance data and the Design data

2.3 Submission of As-Commissioned Microlok Data

The As-Commissioned Microlok Data must be submitted within 5 days of Commission the Microlok into service. The As-Commissioned Data shall be submitted along with all other As-Commissioned documentation drawings as per ESD2503F-05 As-Commission Checklist.

This shall be submitted on CDRom. Separate CDRoms shall be provided for the Maintenance data and the Design data

2.4 Submission of As-Built Microlok Data

The As-Built Microlok Data must be submitted within 35 days of Commission the Microlok into service. The As-built Data shall be submitted along with all other As-built documentation as per ESD2503F-06 As-built Checklist.

This shall be submitted on CDRom. Separate CDRoms shall be provided for the Maintenance data and the Design data

2.5 Microlok Data – Circuit Book Information

A copy of the *Installed Microlok Data Form ESD0511F-02* shall be inserted into the Circuit Book. This shall typically be located as the first sheet in the section with the Microlok configuration drawings. A blank copy of the form shall be included with the As-Designed circuit book. This shall be filled in as part of the testing and commissioning. It shall be verified as part of the As-Built documentation

3 Microlok File Control, Microlok Data Design and Factory Acceptance Testing

3.1 Action

a) Microlok data file names are to be based on the location name and software version. A file extension of .ML2 shall be used. This file is to be a "plain text" file.

E.g. 1682_001.ML2

1682 = Location (e.g. 168.2)

001 = Version

b) A major version may update the tens to a one (e.g. 010).

c) During design the file may be updated as required. Version 000 shall be used.

d) When the data is ready for review, this is noted in the data itself, and the version is incremented to 001. Only data that can be compiled is to be reviewed.

e) The reviewer checks the data and any amendments required are incorporated into the data by the designer, with the version incremented to 002. The reviewer rechecks the altered data. It is permissible for the original version and the revised versions to be compared using CSDIFF to identify the differences.

f) The verifier uses the same process as the reviewer. Any amendments will increment the version number.

g) A"Microlok Project Data Register" shall be kept by the designer. All file versions are to be held in a user directory for that project's data files and included on the register. If work is not carried out on the network (e.g. on a laptop), backup copies are to be made on a USB Hard Drive.

h) Files are to be considered to be 'controlled' from the beginning of the formal review. The register is to be kept on the job file.

i) When the file has been verified, it shall be compiled, and the details of the MLL and MLP files noted on the register.

j) The date and time of the compilation is to be included in the data ML2 file as follows:

- Insert the date and time (say 5-10m in the future) in the file that will be compiled
- Save the file at the appointed time and then
- Compile the file.
- Record the details on the Register.

k) When the initial or altered application is to be installed in the CPU, upload the MLP file and verify the application image in accordance with Section 4.1. Perform the FAT to the test plan, and note any issues on a DTF.

l) At the completion of testing, if necessary, update the data in accordance with 2.4 to 2.9 and retest. Repeat until the data is satisfactory. Sign off the DTF's when that action is complete. DTF's shall be placed on the job file.

m) It will be permissible for review and verification of data altered during FAT to occur after it is ascertained that the FAT is working satisfactorily.

n) Review and verification of changes shall be done before the final FAT conducted by an independent tester. After FAT the tester shall certify the version of data that has been FAT tested on the Data Register Form.

o) The setting of the Microlok address and version need not be finally set until confidence is gained that the data is final, prior to final FAT.

p) On completion of FAT, and at commissioning an "Installed Microlok Data Form" (see Form ESD0502F-01) shall be completed and signed. The certifier must personally confirm the uploaded version and checksums.

q) Data shall not be passed on to unauthorised people without the approval of the Signalling Standards Engineer.

3.2 Cover page

All Engineering documents and Supporting documents are to have a cover page which clearly states the title, version and number of the document.

3.3 Document Status and Amendment Record

All Engineering documents and Supporting documents are to include:

- Document Status indicating the document version (issue and revision), date of version and the relevant authorities for preparation, review, endorsement and approval
- Document Amendment Record which clearly identifies the current version (issue and revision), date of change and outline of the nature of amendment.

3.4 Version Status

The following alpha-numeric indices are to be used for identifying the various stages of Draft, Preliminary, Final, Amended and Reissued documents.

Draft	Issue A – Revisions 0
Preliminary	Issue B – Revisions 0
Final	Issue 1 – Revisions 0
Amendment 1	Issue 1 – Revision 1
Amendment 2	Issue 1 – Revision 2
Reissue	Issue 2 – Revision 0
Amendment 1	Issue 2 – Revision 1 and so on.

3.5 Headers and Footers

Headers and footers are to be used on each page to include the title and number of the document, the version of the document, date of last revision, page numbers and "This document is uncontrolled when printed."

4 Checking Microlok Circuit and Data Design

4.1 Action

a) The following items should be checked during the review and verification of Microlok Circuit Design:

- Check that the correct communications ports are wired out and that any special requirements for the modems, 5V supply, etc, are provided.
- Ensure that the VCOR (Vital Cut Off Relay) cuts vital output functions and signal drivers.
- Ensure CPS down will retain red signal lights.
- Check the card plug couplers are correctly wired for each input or output.
- Ensure card supply (active or negative) is provided on the appropriate cards.

- Ensure that the Microlok II cardfile supply is battery backed, and does not supply external circuits (unless specifically approved).
- Ensure isolated supplies are provided for external circuits.
- Ensure filters/surge protection is in place where circuits go external.
- Ensure diodes are provided across relay coils to suppress noise, when located near cardfiles. Diodes should be as close to the relay coils as physically as possible.
- Check voltage drops on signal lamp drivers for correct cable size and specify the signal lamps supply voltage.
- Check that card plug coupler address jumper settings are correct.
- Check that keying plug locations are correct.
- Confirm card positions in the cardfile.
- Ensure external relays by the Microlok are proven back in to the inputs as per Design standard.
- On non-vital input and output cards, ensure an adequate number of negative return wires are run to carry the current.

b) The following items are checked during review or verification of the Microlok Data Designs;

- Each input allocation is checked against the circuit book. Ensure all external relays by the Microlok are proven back in to the inputs.
- Each output allocation (relay or lamp driver) is checked against the circuit book.
- Each vital or non-vital link shall have the data at either end compared to ensure correct correspondence. Check to the circuit design to ensure the correct ports are connected.
- Each timer is checked for correct time.
- The following systems settings are checked against the details:
    1. Logic Time Out;
    2. Stale data Time Out;
    3. Communications Link Speed.
- Check that the address and the version are correct, and would shut down the cardfile if not.
- Check the vital serial links are shut down with the CPS shutdown
- Check that all vital statements comply with standard data and have all relevant functions included for the geographic arrangement.
- Check that complimentary inputs are crossed proved.
- Check that complimentary outputs are cross proved from the external functions.
- Check that back proving is provided where necessary for the correct sequencing of data evaluation. The following functions are back proved for sequential operation:

    Lock Relays in Lock Relays;

    Approach locking in signal controls;

    Route locking in signal controls;

    Track timers in signal controls.
- The following need not be backproved;
    1. Direction Sticks;
    2. Signal internal HR and DR in track sticks.
- Ensure the version number, date, and compiled time are correct for final data revisions.

- Ensure there are no unused defined Boolean bits.
- Ensure that coded track data has a “dummy” code sent in the absence of any direct code, both ways.
- Ensure coded track codes use “code forcing” to actively drive the codes.
- Ensure that Non-permitted functionality is not used.
- Compile the ‘ml2’ file and check the ‘mll’ to confirm:
    1. No errors
    2. Only permitted warnings for the conversion from vital to non-vital bits exist.
- Record all details on the *Installed Microlok Data Form ESD0511F-02*.

5 Re-Testing of Microlok Data

5.1 Action

a) When the data is altered, a difference file is created between the new data and the previous version using CSDIFF to identify the differences between the two ‘ml2’ files. This file is to be saved as a HTML file to a system driver or if using a laptop in a field situation to a USB Driver.

b) The difference file shall be verified correct by a verifier independent of the designer of the alteration. The verifier need only check the data highlighted as altered. The verifier must also consider whether other changes should also have been made that have not been made.

c) The altered data shall be compiled and uploaded into the Microlok CPU card and then an application software download shall be carried out. The downloaded file shall be given an ‘mld’ extension and saved as a HTML file to a system driver or if using a laptop in a field situation to a USB Driver.

d) The downloaded file is to be reverse compiled and shall be given an ‘mlr’ extension and saved as a HTML file to a system driver or if using a laptop in a field situation to a USB Driver.

e) The Microlok ‘mlr’ file is to be compared with the application software ‘ml2’ file using the Microlok II Application Logic Comparison tool. The resultant file shall be given an ‘mlc’ extension and saved as a HTML file to a system driver or if using a laptop in a field situation to a USB Driver.

f) The Microlok ‘mlc’ file is to be printed and reviewed by the design engineer to ensure all sections of the Microlok data have passed the compilation process.

g) A difference file is to be created using Compare It between the new Microlok ‘mlr’ file and the previous version ‘mlr’ file. Use the Compare It File, Report menu item to run a comparison report and generate a difference file in HTML format.

h) The difference file is reviewed by the designer to ensure the differences are as per those differences identified at section 4.1 a).

i) All details of the newly created ‘mld’, ‘mlr’ and ‘mlc’ files are to be recorded on the *Installed Microlok Data Form ESD0511F-02*.

j) and the reviewed Comparison file and Difference file shall be forwarded to a verifier independent of the designer of the alteration to verify the correct process has been followed.

k) The identified alterations are to be function tested in the Cardfile before placing into service. If the altered data affects the control tables or circuits, these documents need to be amended and verified before testing commences.

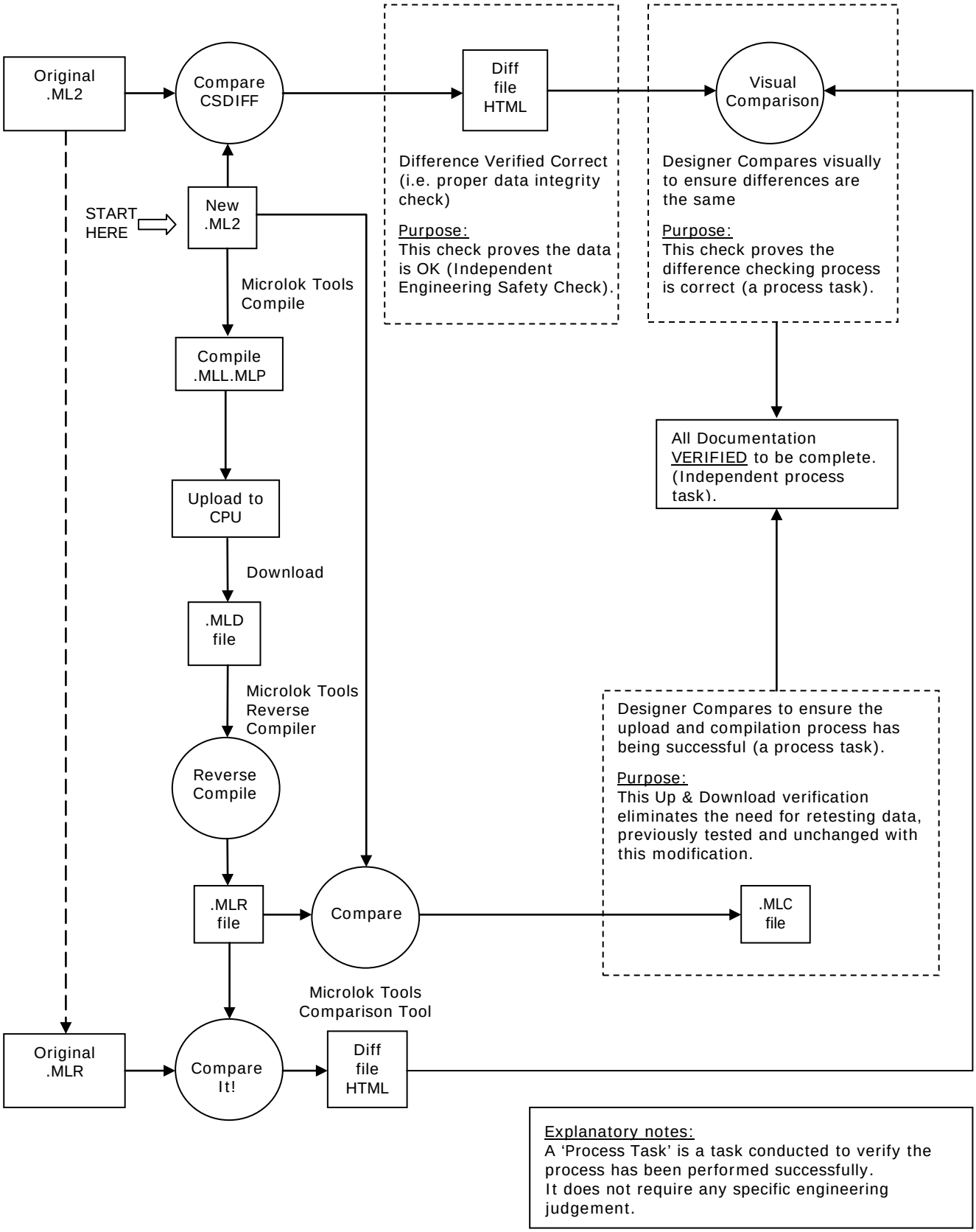
l) The re-test may be conducted on a system set up in Factory Acceptance Test Configuration.

m) The re-test may be conducted by the designer or other tester qualified to conduct a functional test to control tables.

n) The re-test shall be documented by checking off on the control tables or other approved testing plan.

o) The new Microlok data is to be proven operational for a minimum of 20 minutes in the Cardfile prior to being commissioned into service.

p) Control of the data is described in Section 2.1.



6 Appendix A: Request for Microlok II Addresses (example only)

REQUEST FOR MICROLOK II ADDRESSES

Interlocking Locality:		Signal Job No.:	
Commissioning date (proposed):		Project Name:	
Remarks:			

THIS FORM MUST BE SUBMITTED BY THE SIGNAL DESIGN AUTHORITY AT THE COMMENCEMENT OF DATA DESIGN.

Note: Identify all locations that a Microlok II card file is to be installed. The addresses and the Interlocking Number will be allocated and returned to you. A spare address will also be allocated.

Submit form to *Microlokaddress@artc.com.au*

Microlok II Interlocking Addresses		CB No.:	
Interlocking Number:		Interlocking Name:	
Card File Address:		Location:	
Card File Address:		Location:	
Card File Address:		Location:	
Card File Address:		Location:	
Card File Address:		Location:	
Card File Address:		Location:	
Card File Address:		Location:	
Card File Address:		Location:	
Card File Address:		Location:	

Control Systems Interface			
Phoenix Interface:	To		
Phoenix Address:		Location:	
Phoenix Address:		Location:	
Phoenix Address:		Location:	
Phoenix Address:		Location:	
Phoenix Address:		Location:	
Vital Radio data link:		Location:	
Vital Radio data link:		Location:	
Vital Radio data link:		Location:	
Vital Radio data link:		Location:	

Request *(To be signed by the nominated Signal Design Authority or Signal Document Authority)*

I request Microlok II addresses for the above detailed signal works. I agree to provide the ***Installed Microlok Data Form*** immediately after commissioning of the works. All work will be performed in accordance with the ARTC standards.

Signed:	Name:	Date:
Position:	Company:	Tel:

7 Appendix B: Installed Microlok Data Form (example only)

Engineering (Signalling) Procedure - Form
ESD-05-11 Microlok Data Design Records (Addressing, File Control, Checking, and FAT Testing)

Form number: ESD0511F-02

MICROLOK CONFIGURATION DATA FORM

Interlocking Locality: | Signal Job No: | Circuit Book No.:

Commissioned Date: | Project Name:

Remarks:

Location	Compiled File Name	Size (kb)	Date	Time	Address	Version	Check Sum	Application Image CRC	Executive Version	Executive CRC

Example Only

CONFIGURATION CERTIFICATION
(To be signed by the nominated Signal Design Authority or Signal Document Authority)

I certify that the As-Built data detailed above are a true copy of the commissioned signal works. They have been checked and certified. They are in accordance with the ARTC standards.

Signed: | Name: | Date:

Position: | Company:

Maintenance CD attached ☐
Design CD attached ☐

CDrom label must indicate location name and type of files. Each type of file must be in a separate sub-folder on the CDrom.

Version 1.1 | Date of last form revision: 13 August 2010 | Page 1 of 1
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