**Master Signalling Design Resource Plan**

**Signal Design Manager Approved :** Insert Name  **Rail Infrastructure Worker ID**       **Signature ……………………. Date**

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| **Location** |  | | **State** |  | | **Signals Project Type** | |  | | |
| **Design Element** | | **Element**  **ID** | **Designer** | **RIW ID** | **Designer (Mentor)** | **RIW ID** | **Design Checker** | **RIW ID** | **Independent Verifier** | **RIW ID** |
| **Operations Requirements Specification** | | ORS |  |  |  |  |  |  |  |  |
| **Signals Functional Specification** | | SFS |  |  |  |  |  |  |  |  |
| **Signal Plan** | | SP |  |  |  |  |  |  |  |  |
| **Control Tables and Aspect Sequence Charts** | | CT |  |  |  |  |  |  |  |  |
| **Circuits / Circuit Book Number** | | CB |  |  |  |  |  |  |  |  |
| **Track Insulation Plan \*** | | TIP |  |  |  |  |  |  |  |  |
| **Locking Diagrams and Locking tables** | | LDT |  |  |  |  |  |  |  |  |
| **Drivers diagram/Litho** | | DD |  |  |  |  |  |  |  |  |
| **Signal Sighting forms** | | SSF |  |  |  |  |  |  |  |  |
| **Signal Sighting Workgroup Leader** | | SSF |  |  |  |  |  |  |  |  |
| **Detailed site survey (DSS)** | | DSS |  |  |  |  |  |  |  |  |
| **Level Crossing predictor data** | | LXP |  |  |  |  |  |  |  |  |
| **Level crossing monitor data** | | LXM |  |  |  |  |  |  |  |  |
| **Level crossing layout diagrams** | | LXL |  |  |  |  |  |  |  |  |
| **CBI data** | | CBI |  |  |  |  |  |  |  |  |
| **CBI simulator data** | | SIM |  |  |  |  |  |  |  |  |
| **Axle counter data** | | AXD |  |  |  |  |  |  |  |  |
| **Design Element** | | **Element**  **ID** | **Designer** | **RIW ID** | **Designer (Mentor)** | **RIW ID** | **Design Checker** | **RIW ID** | **Independent Verifier** | **RIW ID** |
| **Telemetry data** | | TEL |  |  |  |  |  |  |  |  |
| **Phoenix maps/data** | | PHX |  |  |  |  |  |  |  |  |
| **Power Calculations** | | POW |  |  |  |  |  |  |  |  |
| **Communications data plan** | | CDP |  |  |  |  |  |  |  |  |
| insert other drawing type | |  |  |  |  |  |  |  |  |  |
| insert other drawing type | |  |  |  |  |  |  |  |  |  |
| insert other data type | |  |  |  |  |  |  |  |  |  |
| insert other data type | |  |  |  |  |  |  |  |  |  |
| **Principles Testing on site or in factory** | |  |  |  |  |  |  |  |  |  |
| **Simulator Testing** | |  |  |  |  |  |  |  |  |  |

***NOTES***

***The person nominated as the signal design manager is responsible that appropriately competent persons are allocated to undertake each task.***

***This person shall have a level 2 for Signal Design Management on their SOC.***

***The signal design manager should not undertake the independent verification activities or principles testing but may undertake the design checking activities.***

***A person shall have a level 2 competency in the respective design activity to undertake ‘Checking’.***

***There is no mentoring for ‘Checking’.***

***All elements of the design shall be checked by the signal design manager as being undertaken in accordance with the ARTC Standards and Procedures.***

***Then the signal design manager can endorse as ‘approved’ and submit them to the relevant ARTC project manager.***

***When submitting this form include a copy of the Statement of Competency page 1 for each person listed.***

*\* SA - combined Signal Plan and Track Insulation Plan only.*

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| *Comments:* |
|  |

**Design Elements that are not applicable**

Some of the Design elements listed above may not be applicable or required for a particular signalling project.

If this is the case, they should be listed below and the reason for non-applicability should be detailed.

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| **Design Element** | **Comment on reason for non-applicability** |
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