AUSTRALIAN RAIL TRACK CORPORATION LTD

Discipline: Engineering (Signalling) **Category: Standard**

Design of Microlok II Interlockings

SCP 23

Applicability

New South Wales	✓	**CRIA (NSW CRN)**	✓

Primary Source

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1. Reference Documents

Refer to ESD-05-12 Microlok II Design.

2. System Configuration

2.1. General

Refer to ESD-05-12 Microlok II Design.

2.2. Design goals

Refer to ESD-05-12 Microlok II Design.

2.3. Power supply configuration

2.3.1 General

Power load calculations are to be as per Signal Design quality procedure QSDP 48 Signals Power Design.

2.3.2 High traffic areas

Provide redundant supplies, and design to provide breaks of less than 10mS, with a standalone power supply capacity of 10 minutes or more. Components that are likely to fail within the life of the installation are to have redundant facilities as part of the design.

Normal and emergency supplies must be provided independently from the electricity grid.

Full galvanic isolation is required between each signalling location.

Power distribution should be at extended voltage (that is, higher than 120V).

The power system must detect “brown outs” in the normal supply and then use the other supply.

N+1 redundancy is required for all DC supplies other than track circuits which may use non-redundant DC supplies as per normal practice.

DC power supplies are to be filtered and regulated. However existing unfiltered, un-regulated DC power supplies may be used for external inputs provided that Elsafe immunisation modules (216640) are fitted at the Microlok II inputs.

The Microlok II 12V supply is to be battery backed up as per the Microlok II manuals.

2.3.3 General traffic areas

Supply breaks of up to 30 seconds can be tolerated but should normally be less than 0.1 seconds and occur less than once per 3 month period.

A standalone power supply capacity of 1 minute or more must be provided.

Normal and emergency supplies must be provided from independent sources. The Normal supply must be provided from the electricity grid and a railway supply is preferred.

The emergency supply should usually be provided from the electricity grid. The emergency supply may alternatively be automatically provided by generator, or battery with a 12 hour endurance minimum.

The power system must detect “brown outs” in the normal supply and then use the other supply.

N+1 redundancy is required for all DC supplies other than track circuits, which may use non-redundant supplies as per normal practice for DC supplies that will cause an immediate failure.

Choose approved DC power supplies with a Mean Time Between Failures (MTBF) of greater than 100,000 hours for those DC supplies that do not have redundancy.

DC power supplies are to be filtered and regulated. However existing unfiltered, un-regulated DC power supplies may be used for external inputs provided that Elsafe immunisation modules (216640) are fitted at the Microlok II inputs.

The Microlok II 12V supply is to be battery backed up as per the Microlok II manuals.

2.3.4 Low traffic areas

Supply breaks of up to 60 seconds can be tolerated but should normally be less than 10 seconds and occur less than once per month.

Normal supply can be from electricity grid or solar power. Solar power designs must have a minimum of 7 days autonomy.

Outside the electrified area the emergency supply may be provided by a motor generator, or battery with an 8 hour endurance minimum.

In some cases, not all equipment may be provided with emergency supply (eg point machines), however interlocking equipment must remain functional when operating from the emergency supply.

The power system must detect “brown outs” in the normal supply and then use the other supply.

No redundancy is required for DC supplies. Choose approved power supplies with an MTBF of greater than 100,000 hours.

DC power supplies are to be filtered and regulated. However existing unfiltered, un-regulated DC power supplies may be used for external inputs provided that Elsafe immunisation modules (216640) are fitted at the Microlok II inputs.

The Microlok II 12V supply is to be battery backed up as per the Microlok II manuals.

2.4. Interlocking equipment configuration

2.4.1 High traffic areas

Fully redundant interlocking equipment with non–duplicated external circuits in a hot standby configuration is required.

Inputs from external equipment are commoned and wired to both Interlockings and OR’d together in the interlocking data.

Outputs are OR’d together via facilities to prevent the failure of one system affecting the loads (ie stop “back feeds”).

Disconnection facilities must be provided for testing of new works and alterations without any impact on the operation of the railway.

Direct drive to LED signal lights is currently not permitted as this has the potential to cause the common mode failure of the interlocking equipment.

Individual interlockings may be split vertically if required due to processing constraints. The upper Microlok will process the inputs and interlocking controls to the system, and the lower will process the outputs and comparisons for synchronisation.

2.4.2 General traffic areas

Main interlocking equipment is duplicated in a hot standby configuration.

Interlocking equipment used to interface to track-side equipment does not need to be duplicated.

Direct drive to LED signal lights is not normally permitted as this can cause the failure of the interlocking equipment due to failures of the LED module, however would be permitted where such failures can be shown to be of an impact that fails not more than 2 signals on each track.

Individual interlockings may be split vertically if required due to processing constraints. The upper Microlok will process the inputs and interlocking controls to the system, and the lower will process the outputs and comparisons for synchronisation.

2.4.3 Low traffic areas

The interlocking equipment does not require redundancy for availability.

Direct drive of LED signal lights is permitted. The interlocking design must provide a method to permit disconnection as per the *Microlok Computer Based Interlocking* Signalling Maintenance Procedure SMP 38.

2.4.4 Connection to adjacent interlockings

The preferred connection to an adjacent Microlok interlocking is via vital serial links, making a slave Microlok II location as a slave of both interlocking masters.

The non-preferred connection to an adjacent Microlok interlocking is via vital serial links from Slave Microloks at adjacent locations.

The interface between a Microlok II interlocking and another type of interlocking is via relay style interface circuits.

2.5. Control system communication link configuration

2.5.1 General

Received data may need to be conditioned by the link status as the bit states are maintained when the link fails.

Communications links must have galvanic isolation between the interlocking equipment and any external circuits. Opto-isolators, or transformers are normally used to provide galvanic isolation. Some communications equipment provide galvanic isolation.

2.5.2 High traffic areas

Two fully redundant communication links in constant use, with diverse paths are to be provided.

The communications equipment must use a secure no-break power supply. The communications links must not be disrupted for more than 15 seconds due to power supply disruptions.

Only point-to-point 9600 or 19200 bps, asynchronous, 8 data bit, 1 start bit, 1 stop bit, no parity, full duplex links should be used for main interlockings.

Multi-drop arrangements using Fibre Optic Modems for in-section signalling locations are acceptable, with a point to point link back to the Control System.

2.5.3 General traffic areas

Two communication links are to be provided, a primary and a secondary. The secondary link does not need to be in constant use. If the secondary link is not normally in use then it must be brought into operation automatically, with less than a 90 second disruption to operations. The secondary link must be mostly via diverse path to the primary link. The secondary link must automatically re-establish if it fails whilst in service.

Non-continuous secondary links must automatically disconnect after more than 90 seconds of correct operation of the primary link.

The communications equipment must use a secure power supply. The communications links must not be disrupted for more than 30 seconds due to power supply disruptions.

Point to point 9600 or 19200 bps asynchronous, 8 data bit, 1 start bit, 1 stop bit, no parity, full duplex links are preferred but Multi-drop 9600bps links may be used when point-to-point links are impractical.

2.5.4 Low traffic areas

A single communication link is required with an MTBF of greater than 2 years. A secondary link is desirable. The operation of the secondary link does not need to be automated.

The communications equipment should use a secure power supply. The communications links must not be disrupted for more than 60 seconds due to power supply disruptions.

Point to point 19200, 9600 or 1200bps asynchronous, 8 data bit, 1 start bit, 1 stop bit, no parity, full duplex links are preferred but Multi-drop 9600bps or 1200bps links may be used when point-to-point links are impractical.

2.6. Safety system communication link configuration

2.6.1 General

Safety communication links must not have any buffering or “store and forward” provided in the communications equipment between the Microlok II equipment as per the requirements set out in the Microlok II Platform Safety Application Guidelines.

Typically “dark fibre” or a copper pair is provided and the approved Fibre Optic Modem arrangements, or analogue modems are provided as part of the signalling installation.

Communications links must have galvanic isolation between the interlocking equipment and any external circuits. Opto-isolators, or transformers are normally used to provide galvanic isolation. Some communications equipment provides galvanic isolation.

Particular configuration details are set out in the section on Serial links.

2.6.2 High traffic areas

No single equipment, or cable failure shall cause an operational impact on the railway.

Fibre Optic communications links must be used.

Duplicated point to point links do not require a diverse link but they must have some physical diversity in the links.

Multi-drop links for slaves in more than 5 separate locations must have a loop arrangement with a redundant link. Typically Diversity Link Controllers (DLCs) would be used in this case, otherwise Fibre Optic Modem (FOMs) units would be used.

No more than 10 slave addresses are to be used on one link. This results in a poll cycle time of about 900mS for the link at about 90ms per slave at 19200bps using Fibre Optic Modems.

2.6.3 General traffic areas

Single equipment, or cable failure can cause an operational impact on the railway.

Facilities must be provided so that the Signalling maintenance personnel can correct the failure without other assistance.

Fibre Optic communications links must be used.

Duplicated point to point links do not require a diverse link but they must have some physical diversity in the links.

Multi-drop links for slaves in more than 9 separate locations must have a loop arrangement with a redundant link. Typically Diversity Link Controllers (DLCs) would be used in this case, otherwise Fibre Optic Modem (FOMs) units would be used.

No more than 12 slave addresses are to be used on one link. This results in a poll cycle time of about 1080mS for the link at about 90ms per slave at 19200bps using Fibre Optic Modems.

2.6.4 Low traffic areas

No redundancy for availability is required.

Single equipment, or cable failure may cause an operational impact on the railway.

Fibre Optic communications links should be used for complete new installations. Modem links using copper cables are acceptable when new cable routes are not being provided.

The poll cycle time must be less than 2 seconds.

2.7. Equipment housing and cable route configuration

2.7.1 General

Equipment housings and cable routes must comply with specification alterations identified in the Proposal for Standard Specification alterations to address issues with 415V signalling power distribution, Surge protection installation guideline, and the Ancillary Equipment Temperature rating Installation guideline.

Passive temperature control is required on all locations, using a method of shade structures or “double skinning” and adequate ventilation.

Siting of any location must consider:

- Protection of the location from damage.
- 1 in 100 year flooding.
- Fire risk.
- Surge damage risk.
- Damage due to High voltage power faults.

Location layout must provide:

- Segregation for wiring and equipment for surge protection.
- Layout of equipment and wiring for minimise coupling of electrical noise onto sensitive circuits.
- Layout of equipment for ease of maintenance.
- Layout of equipment for temperature effects.

2.7.2 High traffic areas

A well as complying with the ARTC Signalling Engineering standards requirements for protecting against fire damage and stopping the spread of fire, the limiting of fire damage should be considered in the design.

Passive fire protection should be provided so that cable routes can withstand an external fire without irreparable damage as per SPS 02 Environmental Conditions.

Routing of cable routes is to consider surge protection issues and proximity to High Voltage Earths for Earth Potential Rise (EPR) issues.

Duplicate cables or diverse cables must be physically separated or have appropriate physical protection so that it is improbable that both cables are damaged in the one incident.

Cables that can introduce significant surges must not be placed in close proximity to other cables prior to having passed through some surge protection.

A re-enterable cable route is required.

2.7.3 General traffic areas

Passive fire protection should be provided so that cable routes can withstand an external fire without irreparable damage as per SPS 02 Environmental Conditions.

2.7.4 Low traffic areas

There are no additional requirements for Low traffic areas.

2.8. Microlok specific configuration issues

2.8.1 General

Microlok application data must not use Look-up tables without a specific design guideline being approved for the particular use.

Microlok application data must not use Numeric blocks for purposes other than for configuration control without a specific design guideline being approved for the particular use.

External signalling circuits driven by Microlok Outputs must not have “stick” paths without a design review to confirm that short duration “false” outputs do not cause a hazard.

The LOGIC_TIMEOUT default setting of 2 seconds must be used unless there is a specific problem. It may be set to no more than 4 seconds to address the problem. If this is not satisfactory then other solutions must be found.

The DELAY_RESET default setting is 100mS. It should not normally be changed. It may be set at any value in the provided range to address a particular problem.

The RESET, QUICK.RESET system bits are not to be set by the application logic. The KILL system bit should be used instead.

The SELECTIVE.SHUTDOWN bits for the boards are not to be set by the application logic.

Timers less than 24 seconds can be delayed by more than 10% of their value. Consideration must be given to the impact of delays when using timers of less than 24 seconds. This may cause problems with timers used for speed control.

All direct vital output circuits must be powered via a contact of the VCOR or a repeat of the VCOR.

Safety critical faults detected by the application logic must set the KILL system bit. This shall include the CONFIGURE.ERROR bit.

Vital serial links are to be disabled by the loss of the CPS.STATUS system bit.

It is not necessary to fail a coded track circuit on loss of the CPS.STATUS system bit, however action is to be taken to ensure that track codes are not able to allow a potential safety hazard due to the event that caused the CPS.STATUS to become false.

2.8.2 Approved modules

Part Number	Description	Permitted for High Traffic use	Permitted for General Traffic use	Permitted for Low Traffic use	Notes
N17061301	Central Processing Unit	✓	✓	✓	1
N451232-1701	Microlok 2 Executive Software Revision 5.1	✓	✓	✓	2
N16661203	Power Supply	✓	✓	✓	9
N451910-7501	CPS	✓	✓	✓	
N17060101	Vital Lamp Driver Card	✗	Limited Usage	✓	7
N17060501	Standard Vital Output (12V)	✓	✓	✓	3

N17061001	Vital Input (12V)	✗	Limited Usage	✓	4
N17061003	Vital Input (50V)	✓	✓	✓	4
N17061501	Non Vital Non Isolated Input and Output Card	Limited usage	Limited usage	✓	5
N17061601	Standard 8 Vital Output, 8 Vital Input (12)	✗	✗	Permitted but not preferred	
N17062701	Non Vital Isolated Output Card	✓	✓	✓	
N17063701	Non Vital Isolated Input Card	✓	✓	✓	
N451910-0701	Coded Track Circuit PCBs	✗	✓	✓	8
N17001102	Isolation Module (50V)	✓	✓	✓	6

Notes

1. One spare serial port is to be wired out to interface terminals or a suitable connector.
2. Rev 3.2, Rev 3.4, and Rev 4.01 are approved for continued use but are not to be used on new installations. Alterations should upgrade to Rev 5.1.
3. Spare outputs shall preferably be left unwired. Where future stages will require additional outputs, spare outputs may be wired to interface terminals, and such outputs must be terminated with 220R 1W resistors. All outputs that are wired are to be wired via a disconnect terminal to permit disconnection as per the “Disconnection of Signalling Apparatus” Signalling Maintenance Procedure.
4. Spare inputs may be wired to interface terminals if required for future stages.
5. Only to be used for internal circuits. Care is required in allocating the N12 connections. The input circuits should use A13, C3, C13, C12 as the N12 connections. The output circuits should use A17, A21, A25, A29 as the N12 connections.
6. The isolation module should be provided with 15V power to ensure the output voltage is adequate.
7. Spare outputs may to be wired to interface terminals. All lamps outputs are to meet the requirements for disconnection as per the Microlok Computer Based Interlocking Signalling Maintenance Procedure SMP 38. If the usage is limited then use of the card is permitted based on failure impact meeting the design goals.
8. If permitted, the module is for use in non-electrified areas only. The application data is to contain 75% of the actual track length or a value set by the Engineer certifying the track as the default.
9. This is the Enhanced Power Supply card, launched by US&S as a direct replacement for the old N16660301. The Enhanced card has higher current capacities compared to the old card: 5VDC @ 5A (up from 3A), -12VDC @ 2A (up from 1A), +12VDC @ 1A (unchanged). At time of writing, the Power Calculation in the Microlok Tools software has not been updated, and designers should be aware that this may eliminate the need for external power supplies in some projects.

2.8.3 Timers in High traffic areas

Timers set for less than 24 seconds must be reviewed to determine that they will not cause an operational impact or safety hazard if they are delayed by more than 10%.

2.8.4 Timers in General traffic areas

Based on the lower expected rail traffic conditions Timers set for less than 12 seconds must be reviewed to determine that they will not cause an operational impact or safety hazard if they are delayed by more than 10%.

2.8.5 Timers in Low traffic areas

Based on the lower expected rail traffic conditions Timers set for less than 6 seconds must be reviewed to determine that they will not cause an operational impact or safety hazard if they are delayed by more than 10%.

2.9. Microlok Platform Safety Application Guidelines

Personnel working with Microlok II should be familiar with the *Microlok II Programmable Controller, Platform Safety Application Issues*.

The issues identified in the Microlok II Platform Safety Application issues have been considered and addressed as follows:

Issue	Treatment
1, 2	Signal Design Quality Procedure QSDP16, and QSDP31 to verify the application image
3	Addressed by *Microlok Computer Based Interlocking* Signalling Maintenance Procedure SMP 38
4, 5	Addressed by this document.
6	Design, Review, and Verification on each design.
7, 8	ARTC Signalling Engineering Standards.
9	ARTC Signalling Engineering Standards, and advice from US&S that the Microlok Executive software checks the Boolean logic trigger list as part of the start-up safety checks.
10	Addressed by this document.
11	ARTC Signalling Engineering Standards.
12	Design, Review, and Verification on each design.
13, 14	Addressed by this document.
15	Design, Review, and Verification on each design.
16	Addressed by this document.
17	Addressed by *Microlok Computer Based Interlocking* Signalling Maintenance Procedure SMP 38.
18	Signal Design Quality Procedure QSDP33
19	Design, Review, and Verification on each design.
20, 21, 22, 23	Addressed by this document.
24	Design, Review, and Verification on each design.
25	Addressed by this document.
26	Signalling Maintenance Procedure for MircoTrax.
27	Design, Review, and Verification on each design.
28, 29, 30, 31, 32, 33, 34, 35, 36	Addressed by this document.
37, 38, 39	ARTC Signalling Engineering Standards.
40	Addressed by *Microlok Computer Based Interlocking* Signalling Maintenance Procedure SMP 38
41, 42	ARTC Signalling Engineering Standards.
43, 44, 45	Addressed by this document.
46	Addressed by *Microlok Computer Based Interlocking* Signalling Maintenance Procedure SMP 38.

47	ARTC Signalling Engineering Standards.
48, 49, 50, 51	Addressed by this document.
52, 53, 54, 55, 56	Design, Review, and Verification on each design.
57, 58, 59	Addressed by this document.
60, 61	ARTC Signalling Engineering Standards.
62	Signal Design Quality Procedure QSDP16, and QSDP31 to verify the application image
63, 64, 65, 66, 67, 68, 69	Design, Review, and Verification on each design.
70	Addressed by this document.

2.10. Track side equipment configuration

2.10.1 Signals

2.10.1.1. Direct control by Microlok II

Aldridge

Not currently approved for direct drive by Microlok II Vital Lamp Driver card.

United

The Mark 2 Outdoor 212mm, DC signal light requires a 24R, 25W WH25 series resistor fitted in the signal head when operated using a regulated 16.2V lamp supply.

- Up to 110m cable distance using 1.5mm^2 of twisted pair cable using regulated 16.2V lamp voltage.
- Up to 340m cable distance using 4mm^2 of twisted pair cable using regulated 16.2V lamp voltage.

The Mark 2 Outdoor 212mm, DC signal light requires a 15R, 25W WH25 series resistor fitted in the signal head when operated using an un-regulated 13.6V battery supply.

- Up to 20m cable distance using 1.5mm^2 of twisted pair cable using 13.6V battery supply as the lamp voltage.
- Up to 60m cable distance using 4mm^2 of twisted pair cable using 13.6V battery supply as the lamp voltage.

The Mark 2 Outdoor 127mm, DC signal light requires a 12R, 25W WH25 series resistor fitted in the signal head when operated using a regulated 16.2V lamp supply.

- Up to 110m cable distance using 1.5mm^2 of twisted pair cable using regulated 16.2V lamp voltage.
- Up to 340m cable distance using 4mm^2 of twisted pair cable using regulated 16.2V lamp voltage.

The Mark 2 Outdoor 127mm, DC signal light requires a 10R, 25W WH25 series resistor fitted in the signal head when operated using an un-regulated 13.6V battery supply.

- Up to 40m cable distance using 1.5mm^2 of twisted pair cable using 13.6V battery supply as the lamp voltage.
- Up to 110m cable distance using 4mm^2 of twisted pair cable using 13.6V battery supply as the lamp voltage.

The DC LED stencil indicator requires a 10R, 50W WH50 series resistor fitted in the signal head.

- Up to 110m cable distance using 1.5mm^2 of twisted pair cable using regulated 16.2V lamp voltage.
- Up to 340m cable distance using 4mm^2 of twisted pair cable using regulated 16.2V lamp voltage.

- Up to 20m cable distance using 1.5mm^2 of twisted pair cable using 13.6V battery supply as the lamp voltage.
- Up to 60m cable distance using 4mm^2 of twisted pair cable using 13.6V battery supply as the lamp voltage.

Westinghouse

The RM4 series outdoor, 212mm signal light requires a 15R, 25W WH25 series resistor fitted in the signal head.

- Up to 160m cable distance using 1.5mm^2 of twisted pair cable using regulated 16.2V lamp voltage.
- Up to 450m cable distance using 4mm^2 of twisted pair cable using regulated 16.2V lamp voltage.
- Up to 55m cable distance using 1.5mm^2 of twisted pair cable using 13.6V battery supply as the lamp voltage.
- Up to 160m cable distance using 4mm^2 of twisted pair cable using 13.6V battery supply as the lamp voltage.

The TR3 501 series tunnel or outdoor 127mm signal light requires a 10R, 25W WH25 series resistor fitted in the signal head.

- Up to 160m cable distance using 1.5mm^2 of twisted pair cable using regulated 16.2V lamp voltage.
- Up to 450m cable distance using 4mm^2 of twisted pair cable using regulated 16.2V lamp voltage.
- Up to 40m cable distance using 1.5mm^2 of twisted pair cable using 13.6V battery supply as the lamp voltage.
- Up to 110m cable distance using 4mm^2 of twisted pair cable using 13.6V battery supply as the lamp voltage.

2.10.1.2. Relay control

Relay control of LED signals must be as per the LED signals controlled by relay circuits Design Guideline.

2.10.2 Track Circuits

Track circuit limits are as per the ARTC Signalling Engineering Standards.

2.10.3 Microtrax Coded Track Circuits

The cable from the location to the Microtrax Coded track, track interface unit must be less than 50m of 1.5mm^2 twisted pair cable, or 150m of 4mm^2 twisted pair cable unless a technical review is performed which determines an acceptable feed length for the particular Coded track circuit.

Microtrax Coded track circuits shunting sensitivity is affected by the loop resistance of the cable from the location to the trackside interface unit. The importance of the loop resistance increases as the length of the track increases.

The track interface panel must have RSA disconnect links on the connections to the rails to allow for disconnection as per *Microlok Computer Based Interlocking* Signalling Maintenance Procedure SMP 38 and *Microtrax* Signalling Maintenance Procedure SMP 37.

A 0R22 resistor in the track interface unit is typically fitted in the trackside of the Track Interface unit to decrease the shunting sensitivity to at least 0.25 ohms.

A 0.25 ohm test shunt is used in certifying the Microtrax Coded Tracks.

2.10.4 Relay noise suppression

Relays generate electrical noise when they are de-energised. This electrical noise can interfere with electronic or computerised equipment like the Microlok II.

Relays that are controlled by a circuit that is not exclusively within the location housing the relay are snubbed with a Contact suppressor (RC snubber 0.1uF plus 100R) fitted across the coil. These units are suitable for 12VDC, 24VDC, 50VDC relays. They may be used for 120VAC relays but this will operate the RC snubber at close to its 0.5W power rating. They are available from RS Components as stock number 210-364 for free wiring, and 210-370 with a fixing tab that can be secured under the bottom screw of a Q relay base.

Relays that are controlled by a circuit that is exclusively within the location housing the relay are snubbed with a 1N4007 diode fitted in the reverse direction across the coil. This method is suitable for 12VDC, 24VDC, and 50VDC relays only and it may not be suitable for polarised circuits. Fitting the diode across the relay coil means that the relay cannot be AC immune.

The recommendation in Microlok II manual SM-6400B to use Transorbs is not preferred, as these units have been found to be un-reliable.

In some cases a resistor can also be used for snubbing purposes, this will normally be for an AC circuit.

Relays directly driven by Microlok II must be snubbed.

All relays at a location with Microlok II are to be snubbed or the Microlok II segregated from the source of the electrical noise. The preferred method of segregation is by the use of twisted pair wiring, AC Immunising modules on the inputs, and Microlok II Isolation modules or relays on the outputs and physical separation.

2.10.5 Microlok II input circuits external to the location

Microlok II inputs that are wired external to the equipment location require immunity from sources of 50Hz AC, Traction currents, and general electrical noise as well as surges due to lightning.

Circuits that are wholly within a tunnel and do not travel within 100m of the tunnel portal do not require the surge protection.

The surge protection arrangement must consider 50Hz Earth Potential Rise (EPR) faults if both ends of the circuit are not at the same location.

Two methods are currently accepted for provision of immunity from any source of interference for circuits external to the location.

Method 1

Use Dekoron twisted pair cable and twisted pair wiring with double cut circuits, ensuring that the twisted pair is maintained throughout the whole circuit, and provide a 3 mode surge arrestor (line to line, and line to earth) at any external entry or exit to the equipment location.

Given:

- That the cumulative length of cable route that is within 3m of traction return rails or traction supply wire is less than 100m.
- Power cables that provide power to a load that is more than 10KVA and run parallel to the cable for more than 100m are separated by at least 300mm from the cable.
- Non-twisted cable and wiring does not exceed 3m circuit lentgh.

If the given conditions are not met then the circuit must be treated as per Method 2.

A surge arrestor based on a 290V three terminal ceramic arrestor is considered suitable. The holdover voltage for the arrestor must be greater than 75 volts.

Acceptable external circuit lengths for the 50V input card is 4,000m double cut Method 1 circuit length or 8,000m of wire length.

Acceptable external circuit lengths for the 12V input card is 400m double cut Method 1 circuit length or 800m of wire length.

Method 2 (Only permitted for 50V circuits)

Use traditional signalling cable or wire and Elsafe Immunisation module (216640) near to the Microlok II input.

Twisted pair wiring using the Dekoron cable as per Method 1 may be used.

Note that there cannot be two Elsafe immunisation modules (216640) in series in a circuit for dual Microlok II inputs as there would be a series voltage drop of about 30V across the Elsafe immunisation modules. In this case an Elsafe Gas arrestor (290V) module (216680) is provided at the feed point of the circuit.

The Elsafe immunisation module (216640) provides about 25dB attenuation at 50Hz.

Acceptable external circuit lengths for the 50V input card is 3,000m double cut Method 2 circuit length or 6,000m of wire length.

2.11. Cables and wiring

2.11.1 Colour coding

Generally black wire is used for permanent control wiring. The Power supply wiring colour code is red for positive DC, Black for Negative DC, and Blue for un-earthed AC.

Paired cables or wires for control wirings will normally have black and white as a pair. The white is to be used for the negative or neutral side of the circuit, and black as the Positive or Active side of the circuit.

Some paired cables or wires for control wirings have red and black pairs. The black is used for the negative or neutral side of the circuit, and the red as the positive or active side of the circuit.

2.11.2 General multi-core cable

CBI interface applications may use Olex Dekoron Instrumentation cable with an overall screen for signalling inputs and outputs. The cable must have a nylon jacket and a sacrificial PVC sheath added to the standard cable.

The standard Dekoron cables are twisted pair cables and need to be used as pairs to provide immunity to electrical noise and interference. These cables are permitted for use at voltages up to 130VAC or 150VDC/. Circuit currents should not normally exceed 6 amps, which is half the Manufacture's rated current.

The Dekoron based cable has 1.5mm^2 (7/0.50mm) conductors with an overall screen, in 4 pair, 8 pair, 12 pair, or 24 pair.

Stock Code Cable

001881069 TWISTED 1.5 mm^2, 4 PAIR

001881010 TWISTED 1.5 mm^2, 8 PAIR

001881028 TWISTED 1.5 mm^2, 12 PAIR

001881036 TWISTED 1.5 mm^2, 24 PAIR

2.11.3 Internal Wire

Safety critical wiring in Location cases and Relay Rooms where a Computer Based Interlocking system is being used must use Mil-W-22759-16-16 wire due to problems with the thickness of insulation and the possibility of leaking plasticiser from the standard internal wire as specified in ARTC Engineering Standard SPS 45 *Cables for Railway Signalling Applications - Single Conductor Cables for Indoor Use.*

The wire is available from Cambridge Technologies as part number 16-ACFZ-1929. This is based on the US Military Standard Mil-W-22759-16-16-000.

The wire is also available as black and white twisted pair. Part Mil-W-22759-16-16-0+9 twisted at greater than 15 twists per metre.

This wire is insulated using extruded ETFE, which has good properties for physical abuse during installation, and in service.

The wire is 19/29 AWG, 1.23mm^2 at 15.8 ohms/km. It is rated for 600 volts and 150^{o}C. This wire may be used for safety critical circuits up to and including 120VAC. It is suitable for terminations in general terminals, the 48 way connectors for the Microlok II cardfile, and Q relay crimps.

For 48 way connectors, use twisted pair black & white cable 19/29 AWG, 1.23 mm^2 wires. Use Harting Part No. 09-06-000-8482 crimps for the 1.23mm^2 wire.

The Microlok II CPU 48 way connectors will need connections for serial links. Typically 24 AWG Cat 5 cable is used. Use Harting Part No. 09-06-000-8481 crimps for the 24 AWG Cat 5 cable.

The 96 way connector for the Microlok II non-vital card has insufficient space to use the 1.23mm^2 wire so 19/34 AWG, 0.4mm^2 wire is to be used for the 96 way connector output card, part number Mil-W-22759-16-22-000.

For 96 way connectors, use black 19/34 AWG, 0.4 mm^2 wire. Use Harting Part No. 09-06-000-8484 crimps for the 0.4mm^2 wire.

Stock Code Cable

001881044 TWISTED 1 PAIR (INDOOR CABLE FOR MICROLOK 1.23mm^2)

2.11.4 Heavy duty cable

Heavy duty cable based on Dekoron cable can be used for lamp drive circuits, and coded track circuits.

Stock Code Cable

001887553 TWISTED 4 mm^2 1 PAIR
001887561 TWISTED 4 mm^2 8 PAIR

2.11.5 Power cable for extended voltage Mains

ARTC Stock Code 1901883

> CABLE POWER ELECTRICAL, 16mm^2;
> 2 CORE;7/1.7MM; PLAIN ANNEALED COPPER;
> RED, BLACK PVC/BLACK PVC/NYLON/ORANGE PVC SHEATH;
> 1000M DRUM;

ARTC Stock Code 1901891

> CABLE, POWER, ELECTRICAL, 50mm^2;
> 2 CORE 19/1.78MM PLAIN ANNEALED COPPER;
> RED, BLACK PVC/BLACK PVC/NYLON/ORANGE PVC SHEATH;
> 1000M DRUM;

2.11.6 Fibre Optics

2.11.6.1. General

Multi-mode fibre optic installations are preferred as they are more tolerant to poor environment conditions.

Single-mode fibre optic installations are to have a separate approval for each installation.

2.11.6.2. Cable

Fibre Optic installation must be in accordance to AS-3080:2000 for Fibre Optics.

The multi-mode optical fibre cables shall have a graded-index of 62.5/125 micrometer, with a loss of less than 3.5dB/Km at 850nm.

Fibre Optic cable is to be outdoors type suitable for direct burial, or ducts, and termite resistant.

100% Insertion Loss (light source and power meter) testing of all terminated fibres must be performed in both directions at 850nm for multimode cables.

OTDR tests shall be performed at wavelength used by the Fibre Optic Modems.

2.11.6.3. Fibre Management Enclosure

Terminate Fibre Optic cables in rack mount termination enclosure with patch panel, suitable for a minimum of 16 fibres.

Normally ST or FC connectors are used.

2.11.6.4. Patch Leads

Patch leads are normally Multimode, Duplex, ST to ST, or FC to ST for connection to Fibre Optic modems.

Fibre Optic modems in normal use have ST connectors.

2.11.6.5. Fibre Optic Modems

Currently the only approved Fibre Optic Modem is the OSD136 from Optical Systems Design.

Both single mode and multi-mode versions have been approved.

It is current practice to power the OSD136 from 5VDC via the DB25 connector where practical to reduce the operating temperature of the Fibre Optic Modem.

2.11.6.6. Distance for Multimode fibre

Designs should limit the segments between OSD136 Multimode modems to a maximum of 5 Km of fibre optic cable after allowing for losses in connectors etc.

2.11.6.7. Distance for single mode fibre

Designs should limit the segments between OSD136 single modems to a maximum of 40 Km of fibre optic cable after allowing for losses in connectors etc.

3. Serial Link Communications

3.1. Vital Serial Links

3.1.1 General

All Microlok II vital serial links at: each individual site, and within each section of the cable route, must have a unique serial link address unless they must have identical data because they are individual links of a duplicated link arrangement.

If a Microlok II vital serial link is to operate over cabling or communications multiplexing equipment that extends beyond the trackside signalling cables then an additional 8 bit address must be embedded into the vital serial link data. The application logic must check the additional address and not accept any data unless the address matches the normal address and the additional address.

The Microlok II serial ports have different priorities, port 1 having the highest priority, and port 4 having the lowest priority. Normally the priority of the serial ports will not impact on the design, however if all links are in use, and the CPU is expected to be heavily loaded, it is preferred to allocate the vital links as the lower port numbers.

3.1.2 Fibre Optic Links

These settings are for configurations using Fibre Optic Modems.

3.1.2.1. Master settings

```
LINK:                                   COMMx
ADJUSTABLE ENABLE:                      1
PROTOCOL:                               MICROLOK.MASTER
FIXED PORT:                             x;
ADJUSTABLE BAUD:                        19200;
ADJUSTABLE KEY.ON.DELAY:                30;
KEY.OFF.DELAY:                          12;
STALE.DATA.TIMEOUT:                     4:SEC;
POINT.POINT:                            1;
ADJUSTABLE MASTER.TIMEOUT:              100:MSEC;

ADDRESS:                                xx
ADJUSTABLE ENABLE:                      1
```

STALE.DATA.TIMEOUT default is 4 seconds. It may be decreased or increased to a maximum of 6 seconds to address particular application issues.

POLLING.INTERVAL is normally left at the default and should only be adjusted in response to a particular problem. It should not be set above 200mS.

3.1.2.2. Slave settings

```
LINK:                              COMMx
ADJUSTABLE ENABLE:                 1
PROTOCOL:                          MICROLOK.SLAVE
FIXED PORT:                        x;
ADJUSTABLE BAUD:                   19200;
ADJUSTABLE KEY.ON.DELAY:           30;
KEY.OFF.DELAY:                     12;
STALE.DATA.TIMEOUT:                4:SEC;
POINT.POINT:                       1;
INTERBYTE.TIMEOUT:                 0:MSEC;
ADDRESS:                           xx
ADJUSTABLE ENABLE:                 1
```

STALE.DATA.TIMEOUT should not be changed from the default of 4 seconds. It may be increased to a maximum of 6 seconds to address particular problems.

3.1.3 Analogue Modems

Modems must have controlled carrier with a carrier startup time of less than 280 bit times. Typically at 9600 bps the carrier startup time is less than 30mS. Most modems are not suitable.

The Exicom 396 modem is approved for Microlok 2 vital serial links.

The Dataplex 210 short haul modem specifications are suitable, however the modem has not been tested at the time of writing.

3.1.3.1. Master settings

```
LINK:                              COMMx
ADJUSTABLE ENABLE:                 1
PROTOCOL:                          MICROLOK.MASTER
FIXED PORT:                        4;
ADJUSTABLE BAUD:                   9600;
ADJUSTABLE KEY.ON.DELAY:           280;
ADJUSTABLE KEY.OFF.DELAY:          20;
STALE.DATA.TIMEOUT:                4:SEC;
ADJUSTABLE MASTER.TIMEOUT:         250:MSEC;
POINT.POINT:                       1;

ADDRESS:                           xx
ADJUSTABLE ENABLE:                 1
```

MASTER.TIMEOUT should be set at 250mS and may be increased to 500mS to address particular problems.

STALE.DATA.TIMEOUT should not be changed from the default of 4 seconds. It may be increased to a maximum of 6 seconds to address particular problems.

POLLING.INTERVAL is normally left at the default and should only be adjusted in response to a particular problem. It should not be set above 200mS.

3.1.3.2. Slave settings

```
LINK:                                COMMx
ADJUSTABLE ENABLE:                   1
PROTOCOL:                            MICROLOK.SLAVE
FIXED PORT:                          x;
ADJUSTABLE BAUD:                     9600;
ADJUSTABLE KEY.ON.DELAY:             280;
ADJUSTABLE KEY.OFF.DELAY:            20;
ADJUSTABLE STALE.DATA.TIMEOUT:       4:SEC;
ADJUSTABLE POINT.POINT:              1;

ADDRESS:                             xx
ADJUSTABLE ENABLE:                   1
```

POINT.POINT is set to 1 unless multi-drop analogue modems are used.

Baud is set to 9600 unless a particular modem's limitations require a lower speed.

3.1.3.3. Exicom 396 modem settings

The modem needs to be configured for V.29 fast train, 9600bps, Half Duplex, Asynchronous, 10 bits/Character.

The modem can use 4 wire or 2 wire communication links. 4 wire communication links are preferred.

Switch 1/1 ON Links S, and T Don't Care	Primary rate.
Switch 1/2 ON Don't Care	
Switch 1 /3 ON	
Switch 1/4 ON	V.29 fast train
Switch 1/5 OFF Don't Care	
Switch 1/6 OFF	- 10dbm
Switch 1/7 OFF	-26dbm receive
Switch 1/8 OFF Link L installed, Link K out.	Internal clock
Switch 2/1 ON Link D installed, Link C out for 2 wire or Half duplex.	
Link C installed, D removed for 4 wire.	
Switch 2/2 OFF	Point to Point.
Switch 2/3 OFF	No squelch
Switch 2/4 OFF	No RTS delay
Switch 2/5 OFF	No retrain
Switch 2/6 OFF	not used for this mode.
Switch 2/7 OFF	not used for this mode.
Switch 2/8 OFF	not used for this mode.
Links N installed, M removed	Pin 9 isolated
Links R installed, P removed	Pin 10 isolated
Links A installed, B removed.	600 ohm receiver.
Switch 3/1 OFF	Don't Care
Switch 3/2 OFF	Don't care
Switch 3/3 OFF	No link amplitude equalizer.
Switch 3/4 OFF	No receive delay equaliser
Switch 3/5 OFF	No cable equalizer.
Switch 3/6 OFF	No cable equalizer.
Switch 3/7 OFF	No digital delay equalizer.
Switch 3/8 ON	Ccts 140, & 141 disabled

Links G installed, H removed.	
Links E installed, F removed.	
E-link removed	Signal ground isolated from protective ground.

Switch 4/1 OFF	10 bits per character.
Switch 4/2 OFF	
Switch 4/3 OFF	Async timing at Basic tolerance.
Switch 4/4 ON	Asynchronous

605 Plug terminals	4W TX 2, 3, and RX 4, 6.
2W TX/RX 4,6	although document implies 2/3 is expected.

Configuration

Design to provide a received signal levels to modems of at least 10dB above the minimum modems receive level.

Typically 5 km between modems is easily achieved.

3.1.4 Circuits

RX:	Wire to Communications device or other Microlok port TX of the Microlok port.
TX:	Wire to Communications device or other Microlok port RX of the Microlok port.
DCD:	Wire to Communications device or other Microlok port RTS of the Microlok port.
RTS:	Wire to Communications device or other Microlok port DCD of the Microlok port.
CTS:	Hold in the OFF state.
Modem DTR:	Line should be held in the ON state for analogue modems, but may be left unused for Fibre Optic Modem.

3.1.5 Conversion between RS485 and RS232

The Alfatron A440 RS232-RS422 converter is approved for use on Microlok Vital Serial Links. The Alfatron A440 is used because it provides the RTS, and DCD control links as well as the TXD, and RXD.

The Alfatron A440 does not provide galvanic isolation. Careful consideration is required in the choice of power arrangements for the Alfatron A440 and other serial communications equipment to ensure the installation is not exposed to surges via the serial communications link.

3.1.6 Wiring

Category 5 telecommunications cable using 24 AWG wire may be used for RS485 wiring within the location or building.

Category 5 telecommunications cable using 24 AWG wire may be used for RS232 wiring within the location or building to a maximum length of 5 metres.

RS232 wiring up to 15 metres is permitted using shielded cable designed for RS232 applications.

The twisted pair ETFE Teflon internal wire may be used for RS485 wiring for distances up to 5 metres.

3.2. Genisys links (Control system link)

Genisys requires an asynchronous communications link with 8 data bits, no parity, 1 start bit, and 1 stop bit with speed (in order of preference) of 19200 or 9600 bps. Where the communications line quality is low, 1200 bps may be used if a reliable connection cannot be established at 9600 bps.

Depending on the configuration the primary link is:

- Full duplex leased line modems at 19200, or 9600 bps or
- A full duplex Telstra DDS (Direct Data Service) operating at, 19200 or 9600 bps;

and the secondary link is:

- A full duplex,19200, or 9600 bps leased line modems; or
- Dial-up modems set for full duplex, 9600 bps.

External switching between primary and secondary links can be performed by Black box SW111AE RS232 Fallback switch.

3.2.1 Slave

These settings are for Genisys slaves of either ATRICS or Phoenix Control System masters using point to point direct connections or Modems.

```
LINK:                                COMMx
ADJUSTABLE ENABLE:                   1
PROTOCOL:                            GENISYS.SLAVE
FIXED PORT:                          x;
ADJUSTABLE BAUD:                     19200;
ADJUSTABLE STALE.DATA.TIMEOUT:       15:SEC;
ADJUSTABLE CARRIER.MODE:             CONSTANT;
ADJUSTABLE POINT.POINT:              1;

ADDRESS:                             xxx
ADJUSTABLE ENABLE:                   1
```

3.2.2 Master

The Master Genisys arrangement would only be used where a Microlok is acting as the control system, for example, a push-button panel with a Microlok providing the non-vital interface between the panel and the interlocking. The settings shown are for the panel interface communicating with a single-sided interlocking master.

```
LINK:                                COMMx
ADJUSTABLE ENABLE:                   1
PROTOCOL:                            GENISYS.MASTER
FIXED PORT:                          x;
ADJUSTABLE BAUD:                     19200;
ADJUSTABLE STALE.DATA.TIMEOUT:       15:SEC;
ADJUSTABLE CARRIER.MODE:             CONSTANT;
ADJUSTABLE MASTER.TIMEOUT:           300:MSEC;
ADJUSTABLE POINT.POINT:              1;

ADDRESS:                             xxx
ADJUSTABLE ENABLE:                   1
```

Where a dual hot standy interlocking is used, STALE.DATA.TIMEOUT must not be set to more than 2 seconds, in order for the hot standby changeover to work.

3.2.3 Circuits

RX:	Wire to Communications device or other Microlok port TX.
TX:	Wire to Communications device or other Microlok port RX.
DCD:	Wire to Communications device or hold in the ON state.
RTS:	Normally leave disconnected unless using Multi-drop communications or Half-duplex modems.
CTS:	Hold in the OFF state
Modem DTR:	Should normally be held ON.
Modem RTS:	Should normally be held ON.

3.2.4 Conversion between RS232 and RS485

The Adam 4520 RS232-RS485 converter is approved for use in Genisys Serial Links.

The Adam 4520 provides galvanic isolation on the serial link. The preferred use is for the Adam 4520 to be powered from the Microlok II B12/N12 supply, and the RS485 side is connected to the Microlok II serial port.

The Adam 4520 is normally left in its default settings of 9600bps, 10 bit. The RTS line on the RS232 interface must be held ON.

3.2.5 Wiring

Category 5 telecommunications cable using 24 AWG wire may be used for RS485 wiring within the location or building.

Category 5 telecommunications cable using 24 AWG wire may be used for RS232 wiring within the location or building to a maximum length of 5 metres.

RS232 wiring up to 15 metres is permitted using shielded cable designed for RS232 applications.

The twisted pair ETFE Teflon internal wire may be used for RS485 wiring for distances up to 5 metres.

3.2.6 Modem Configuration

The modem currently preferred by Engineering Standards and Services Signals for the non-vital link is the Westermo TD-35LV. When interfaced to ATRICS, Communications & Control Systems will specify different modems.

The TD-35 is designed for industrial use and incorporates several features to facilitate reliable operation, including:

- Low supply voltage – can be powered directly from the battery-backed 12V Microlok supply, ensuring that the modem works even if the 120V supply is lost, and no step-up transformer is required;
- Full galvanic isolation of all ports, including the power supply connection;
- Watchdog function monitoring hardware, software, and power supply. In the event of internal fault, the watchdog will reset the modem enabling communications to be restored automatically;

The modem also provides DIP switches which can be used to set many of the operating parameters of the modem without requiring a computer to initialise the AT commands. Refer to the TD-35 manual for the location of the switch groups in the modem.

3.2.6.1. Leased Line Settings

Switch Group	Genisys Master end	Genisys Slave end
SW1	1 – 2 ON (Leased line answering)	1 off, 2 ON (Leased line calling)
	3 – 8 off	
SW2	1 – 3 ON, 4 off (19200 baud) OR 1 off, 2 – 3 ON, 4 off (9600 baud)	
	5 – 6 ON, 7 off (8 data bits, No parity) 8 off (1 Stop bit)	
SW3	1 – 2 off, 3 ON, 4 – 8 off (sets commonly used AT parameters)	
SW4	1 – 4 ON (automatic line speed) 5 – 6 off 7 ON (4-wire mode for leased line) 8 off	

When using the modems on a leased line, all of the modem configuration can be achieved by use of the switches.

For leased line operation, 4-wire is preferred. Where problems are experienced, 2-wire mode may be used by setting SW4-7 off, and changing the telephone line connections appropriately. The telecommunications service provider should be contacted to arrange to have the problems investigated and corrected.

3.2.6.2. Dial-up Settings

Switch Group	Genisys Master end	Genisys Slave end
SW1	1 – 2 off (PSTN dial-up) 3 – 8 off	
SW2	1 – 3 ON, 4 off (19200 baud) OR 1 off, 2 – 3 ON, 4 off (9600 baud)	
	5 – 6 ON, 7 off (8 data bits, No parity) 8 off (1 Stop bit)	
SW3	1 – 2 off, 3 ON, 4 – 8 off (sets commonly used AT parameters)	
SW4	1 – 4 ON (automatic line speed) 5 – 8 off	

For dial-up operation, the interlocking end will normally be the dialling modem. A fallback switch will detect failure of the primary link, and trigger the modem to dial by asserting the DTR line to the modem. A computer must be used to configure the dialling settings for the modem using the command string AT&A1&B1&D3S0=0&Z0=n (where n is the phone number the modem is to dial). The modem at the control system end must be configured by computer with the command string AT&A1S0=2. Instructions should be provided in the circuit book and the maintenance instructions. Because the TD-35 has two connection options for the RS-232 port, the maintenance instruction must also include a warning to ensure the Microlok is disconnected from the modem before a computer is connected to the modem.

Modem AT commands used:

&A1	Ignore characters from the computer / Microlok during the call establishment phase
&B1	Dial the stored number when DTR line rises
&D3	Perform soft reset when DTR line falls
S0=x	Auto-answer after x rings (zero disables auto answer)
&Z0=n	Store the phone number n in phone number memory 0

3.3. Control line states

3.3.1 RS232 Control Lines

OFF state for control lines is –12V.

ON state for control lines is +12V.

3.3.2 RS422/RS485 Control

OFF state for control lines is –ve terminal to 0V, +ve terminal to +5V.

ON state for control lines is –ve terminal to +5V, +ve terminal to 0V.

3.3.3 RS423 Control

OFF state for control lines is –6V.

ON state for control lines is +6V.

Note that the link setting for port 3 is normally set for RS232 so although port 3 is described as RS423 it is normally configured as a RS232 port.

4. Application Logic Design

4.1. Introduction

The Microlok II development system tools are to be used to develop and compile an application logic program, debug the program, and upload the application program to the Microlok II central processing unit (CPU) card.

For the comprehensive procedures to create the complete Microlok II application program, reference should be made to the US&S Microlok II System Application Logic Programming Guide. SM-6800D manual.

The application logic is to be designed in accordance with the Signal Design Quality Procedures QSDP16: Microlok File Control, Microlok Data Design and Factory Acceptance Testing, QSDP31: Retesting of Microlok Data, QSDP33: Checking of Microlok Circuits and Data Designs.

Design Engineers are to ensure the application logic is produced utilising the current approved Microlok II development tools and compilation software.

In general the application logic is based on or derived from the Signalling Circuit Design Standards. It is important to note all the features that can be programmed into the Microlok II system but are not or cannot be part of current relay design methodology, and the features that are part of current relay design methods which are not essential or necessary for the satisfactory operation of computer based interlockings and non-vital equipment.

Typical examples of these are:

- Replication of magnetically latched relays in principle.
- Removal of back contact proving for relay down proving purposes only.
- Removal or addition of relay features not relevant to ‘software’ relays.
- Specific maintenance indications and diagnostics.
- Timing and indication features that would be an expensive addition to conventional systems.

4.2. Design Process

The following steps should be followed when producing Microlok II application designs.

- The Design Engineer identifies the system configuration requirements such as the Microlok II circuit boards to be used, system interconnects, vital and non-vital I/O requirements, and all required interlocking logic.
- The application logic is created utilising a standard text editor to create the data file. It is recommended that NOTEPAD+ be used for this purpose. This file is given a filename extension of “ml2”
- The Microlok II logic compilation software is to be used to process the completed application logic data file. The compilation software produces an application source file (mlp extension) and a listing file (mll extension). The listing file contains a summary of the application program, as well as any errors detected in the source file.
- The application logic file may need to be corrected using the text editor and run through the compiler again.
- The compiled application source file may be uploaded to the appropriate Microlok II cardfile installation utilising the Microlok II Maintenance Tools program.

4.3. System Limitations

- There can be no more than 4095 assign statements in the Boolean Logic section. This includes the total number of ASSIGN and NV.ASSIGN statements and the timer bits. Where the number of assign statements exceeds 3000, or the number of defined bits exceeds 3500, the system may become heavily loaded. Designers will need to pay particular

attention during testing to ensure that the system will be stable, and alternative configurations may need to be considered.

- There is a combined limit on the number of timers, tables, and numeric blocks that may be defined, this limit is 399.
- A single ASSIGN or NV.ASSIGN statement may assign to no more than 32 bits.
- A bit used in the output list of an assign statement may trigger no more than 50 assignments, tables, blocks, or coded outputs.
- A maximum of 499 statements can be awaiting execution at any time on each of the execution queues for ASSIGN and NV.ASSIGN statements.
- A maximum of 128 data bit inputs and 128 data bit outputs, per address may be defined for transmission over a vital serial link. (Microlok Protocol)
- A maximum of 512 data bit inputs and 512 data bit outputs, per address may be defined for transmission over a non-vital serial link. (Genisys Protocol)

4.4. Standardisation of OCS Control of Interlockings

4.4.1 Background

Entrance – exit style interlockings in NSW have developed over the years and have a number of features and constraints in the design.

Some of these have resulted from a system that was developed from using magnetically latched RLR relays for signal routes, and thermal approach locking release timers, which required an (N)R function, and circuits using direct button interfaces on the control panel.

For new works, the NX style of circuit philosophy is to be largely replaced with the OCS style.

This will simplify the data design, improve operational flexibility, and present a more appropriate interface to the present control system.

4.4.2 Applicability

This is applicable to new Microlok interlocking projects that interface to both Atrics or Phoenix and should be generally applicable to all control systems.

It may not be directly applicable to existing installations where an NX control panel is retained, although existing relay based systems could be modified to provide this approach.

4.4.3 Elements of the OCS Philosophy

The original OCS type installations had the following features:

- An RSR relay (Non-vital) that incorporated the lever stick function.
- Drop track circuit releasing in Approach Sticks for shunts only.
- Non storage of point controls individually applied to each set of points.
- Locking arrangements that did not require point sequencing for overlap maintenance as a result of the simple layouts.
- Route normalisation calls initiated on the ‘A’ track down.

The operational implications of these arrangements include:

1. When shunting on main aspects, the ALSJR timer is used to normalise routes.
2. It is not possible to maintain a route set if the ‘A’ track is failed.

4.4.4 Elements of the NX Philosophy

Entrance exit systems are generally used only in the larger interlockings and is the usual form of interlocking in the metropolitan area.

The following features are typical:

- Machine in Use/Finish function to advise the signaller of the status of the commence and finish of each route.
- A restriction of being able to only set one route at a time.
- Track down releasing of Approach Locking.
- TZR/NR functions for automatic normalising that protect against a common, mode failure releasing locking in the face of a train.
- Availability functions for point sequencing.
- Non storage of points implemented through the 'one shot' route setting command requiring points to be free or available at the time of setting.
- Control System commands are pulsed.

The operational implications of this arrangement include:

- Can only set one route at a time.
- Shunting requires the signaller to manually cancel the route as the auto normalising does not operate when the berth track is occupied.
- It is (usually but not always) possible to set routes over track failures.

4.4.5 Changes to Interlocking Philosophy

The following changes to the current standard NX interlocking will occur:

- An RSR be provided for route setting and normalisation.
- The RSR not to stick if the NLR does not drop at time of setting.
- The non-storage feature be retained using the UJZR function inherent in the way Microlok Booleans provide for the NLR.
- Route normalisation to be initiated by the 'A' track dropping the RSR.
- Because the route normalisation is initiated by the 'A' track dropping the RSR, drop-track releasing has to be modified to minimise the risk of a single failure normalising the route prematurely.
- The following functions be removed:
  - Ring circuit
  - Commence and Finish relay
  - Machine is Use relay
  - TZR
  - NR
  - SR

  A modified TZR is used in the new approach locking release arrangements.
- Data to provide for separate main (120s) and subsidiary shunt (60s) approach locking release times and approach stick relays be provided to simplify current approach locking data.

The technical and operational implications of this arrangement are:

- A consistent and identical interface for ATRICS and Phoenix. (Phoenix may not utilise all the indication bits).
- Ability to set non-conflicting routes simultaneously. (Note: The Control System must prevent the issue of simultaneous calls on conflicting routes to prevent possible lock-outs occurring in the interlocking)
- Considerably simplified route normalising data without loss of safety integrity, which will reduce data design time and simplify the checking process.

- Consistent route normalisation when the signal is passed irrespective of whether the approach tracks remain occupied, without signaller intervention required by cancelling the route.
- It will not be possible to set a route (especially a shunt route) if the 'A' track is failed. (However the track replacement in the RSR can be omitted for non track controlled signals)
- In some areas, approach locking time releasing will be required, possibly delaying route cancellation, during shunting.
- Point sequencing will operate as per the current NX relay interlockings.

4.4.6 Further Enhancements to the Interlocking Philosophy

Generally, the operational disadvantages are not considered to adversely affect train operation or system operation. In some cases, it may be an operational requirement to be able to set a route when the 'A ' track is occupied. In this case, the following techniques are available:

1. Using the berth track down in lieu of or in parallel with the 'A' track to hold the RSR. The route would then cancel when the train has fully passed the signal. It would only be possible to set the route when the train has occupied the berth track with the 'A' track down. This arrangement would not be universally applied and hence signallers may have difficulty in knowing which routes had this facility.
2. Using ATRICS or Phoenix and maintaining the control system call until the signaller manually cancels the route (this could be performed, by using an additional button similar to the Emergency Shunt Function button).

   Option 2 is preferred as it results in the data design not requiring any modification from standard, and would provide for a more consistent user interface.

   Deliberate signaller selection to clear a shunt signal without first track replacement is a requirement of the Emergency Shunt Function. This arrangement could be universally applied.

   The route availability for the shunt signal (but not the ESF) in the control system will need to include the 'A" track to prevent the signal momentarily clearing and replacing during route calls with the 'A' track occupied. Pending this facility being introduced, shunt route checking data should include the 'A' track.

   Option 2 would permit the design of interlockings to a consistent standard, and future upgrades of ATRICS only would then be able to retrospectively introduce this facility. The same method could also be used for auto-reclearing of main routes.

   Variations between ATRICS and Phoenix Implementation

   Within Phoenix systems there is no necessity to prove the route NLR down in the RSR stick path, as the route set indications are produced by the Phoenix itself and an out of correspondence between the RSR and RUR would be seen as a failure prompting the signaller to cancel and reset the route.

   Within ATRICS however, the interlocking drives the display and there is a possibility that the RSR could be up with the route unset and UJZR down. There would be no indication that the route needs to be cancelled and reset. To ensure this does not occur a back contact of the route NLR needs to be provided in the stick path of the RSR to ensure the RSR does not remain up if the route does not set.

4.5. General Guidelines

The Microlok II boolean logic section of the program does not execute in the same manner as a typical computer program. A Microlok II program only executes those ASSIGN or NV.ASSIGN statements that need to be re-evaluated based on changes.

The Microlok II boolean logic also follows a 'break' before 'make' rule.

4.5.1 Program Title

Every Microlok II program is to be provided with a title name. This name is to be consistent with the signalling location that the interlocking is to be installed.

4.5.2 Address Allocation

Every Microlok II cardfile is to be provided with an address number. This number must be unique to the area or region to which that cardfile is to be installed.

In configurations where one 'Master' Microlok II interlocking is communicating with multiple 'slave' cardfile locations an interlocking address number is also to be provided. Reference should be made to the Hot Standby Arrangements document in the appendix for how the address numbers are utilised in the application logic design in this instance.

Allocation of the address is made through the Microlok Address Register in the Signal Design Office.

4.5.3 Naming Conventions

Where possible bit names are to be kept the same as those used in conventional relay interlockings.

Bits defined in the interface section as inputs or outputs for a serial link are usually prefixed with the serial port number, for example: 3_100MA_HR.

As a general rule, the trailing 'R' (denoting 'relay') is not required on data names.

Reference should also be made to the relevant Microlok II manual to ensure reserved words and system bit names are not used.

4.5.4 Hot Standby

Where the interlocking configuration requires a Hot Standby arrangement, reference should also be made to the document 'Microlok II – Dual Hot Standby Arrangements'. A copy of this document can be found in the appendix.

4.5.5 Interface Section

The interface section defines all of the local and serial I/O bits for the Microlok II cardfile.

Up to 6 serial links may be declared in an application program although only 4 may be enabled at any one time. (There are 4 physical serial ports available)

4.5.6 Boolean Bits

Any bits that are assigned to a function that is exclusively used within the application logic and is not defined as either an input or output bit in the interface section is defined as a boolean bit.

In a typical program, a boolean bit is equivalent to a relay coil that is not an input or output.

4.5.7 Timer Bits

Defining timer bits is equivalent to making relays slow to pick, slow to drop, or both. Any boolean bit or output bit can be given timing characteristics.

All timers may be defined as "adjustable" excluding those used for safety critical purposes.

4.5.8 Log Bits

The Microlok II includes a built in event recorder. Any of the bits used in the program can be logged.

Care must be taken to ensure any bits that flash or pulse are not logged.

It is also necessary to log some of the internal system bits, inclusive of the following: LINK_3.ENABLED, LINK_3.33.Status, (serial link bits for port 3, address 33)

RESET, QUICK.RESET, KILL, CPS.ENABLE, CPS.STATUS, LOG.LARGE, LOG.FULL, LOG.OK;

It maybe noticed that the Microlok performance seems to slow down on occasions, this may be when the system is writing a "snapshot" to the log.

US&S have received reports about the event logger causing a load on the system. Upon further investigation, they have found that the user has specified every bit to be logged in the system data. For large applications, this can cause a loading problem.

Snapshots are logged when "too many" bits change at the same time. Too many is defined as the "total number of bits being logged" divided by 5, with a minimum of 50 and a maximum of 100.

So, if 300 bits are being logged, if more than 60 (300/5) bits change at the same time, a snapshot is logged. If 55 bits change at the same time, they are logged individually.

Also, the system always makes sure that at least 1 snapshot is present in the log.

As a minimum, the bits to be logged are:

- All inputs (vital and non-vital)
- All outputs (except flashing, pulsing or toggled outputs)
- Any internal bit that may give a concise report of an event. As a general rule logging of all internal variables is not required. Internal bits that initiate flashing, pulsing or toggled outputs are to be logged.

4.5.9 Boolean Logic

The basic format of an assign statement is:

ASSIGN (or) NV.ASSIGN <boolean expression> TO <bit>;

The operators used in the boolean expressions in order from highest to lowest precedence are as follows:

~ ,	! ,	NOT	Boolean NOT
* ,	& ,	AND	Boolean AND
+ ,	OR		Boolean OR
@ ,	^ ,	XOR	Boolean XOR

Operators of the same precedence are evaluated from left to right, and using parenthesis may change operator precedence.

Parenthesis should be kept to a minimum, however if there is any doubt with complex ‘or’ statements, they should be used to ensure designers and checkers have a clear understanding of the way the Boolean will function.

Where data constructs have a number of complex parallel paths, consideration should be given to breaking up the data so that it is more readable.

COMMENTS

Comments can be placed almost anywhere within the program.

Comments are notes which would add clarity to the data reader and are ignored by the compiler. Liberal use of comments are encouraged to make the program easier to understand.

4.5.10 Constants

Constants that are to be used in the program are to be defined. Typically this is done as follows:

```
CONSTANTS BOOLEAN

TRUE = 1;

FALSE = 0;
```

4.5.11 Conditional Power Supply Logic

The internal system bit, CPS.ENABLE is used in the control of the VCOR relay, as long as all diagnostics are passed the VCOR relay will always pick.

Typically this is done as follows:

```
ASSIGN TRUE            TO       CPS.ENABLE;
```

4.5.12 Vital Serial Ports

Where serial port configurations exist that utilise the vital “MICROLOK” protocol, these ports are to be disabled should the Microlok II cardfile CPS status be down.

Typically this is done as follows:

```
ASSIGN                 ~CPS.STATUS                 TO LINK_3.DISABLE;
```

Where serial links are in use there may be a requirement to prove the link is operational before allowing certain bits to become true, for example input control bits received over a non-vital link. Where this function is required a boolean bit may be defined with a name particular to that serial link, for example LINK_3.

Data having inputs from Genisys serial links should have a Comms link status bit included so that Genisys bits that freeze on link failure or disconnection will not affect system operation, if paired internally with a backup or duplicated link.

The LEDs on the front of the Microlok II CPU card are also generally utilised to indicate to the Maintenance staff the status of serial links.

Typically this is done as follows:

```
// SERIAL LINK MONITORING LOGIC

ASSIGN                 LINK_3.33.STATUS            TO LINK_3;

NV.ASSIGN              LINK_3.33.STATUS            TO LED.3;
```

4.5.13 Program Verification Logic

In order to ensure the correct version of application logic is uploaded into the Microlok II cardfile location, program verification logic has been developed. This logic also ensures the version of the compilation software is verified to the executive version of software loaded into the Microlok II CPU card.

The statements listed in the User Numeric section of the program work in conjunction with the program verification logic to ensure the correct numbers are entered during the modification of the system configuration settings. If the incorrect numbers are entered at this time the Microlok II unit will shutdown due to the internal system bit “KILL” becoming true.

Note that “KILLZ” is a boolean bit.

The program verification logic and User Numeric are as follows:

```
USER NUMERIC
ADDRESS_NUMBER :                "Set Address Number" ;
REVISION_NUMBER :               "Set Revision Number" ;
EXECUTIVE_VERSION:              "Set Executive Version" ;


ASSIGN KILLZ + CONFIGURE.ERROR TO KILL;

END LOGIC
NUMERIC BEGIN

//PROGRAM VERIFICATION LOGIC

BLOCK 1 TRIGGERS ON CPS.ENABLE AND STALE AFTER 0:SEC;

ASSIGN (ADDRESS_NUMBER <> 89) OR (REVISION_NUMBER <> 5) OR
(EXECUTIVE_VERSION <> 510)                          TO KILLZ;

END BLOCK

END NUMERIC
```

4.5.14 Revision Number Verification

Where the Microlok II application logic has been produced for the MASTER interlocking of a Hot Standby configuration revision verification logic is to be provided. This logic is to be produced to ensure identical data is uploaded into both of the two MASTER interlocking cardfiles. The logic converts the revision number into a 4 digit binary number, which is then passed through the dual link of the Hot Standby configuration and compared with the revision number of the other interlocking. If the two compared numbers are not identical the internal system bit “KILL” will be made true causing the Microlok cardfile to shutdown.

An example of revision verification logic is as follows:

```
//REVISION NUMBER VERIFICATION LOGIC

ASSIGN     ~DUAL_LINK_OK + (I2_REVISION_BIT1 * REVISION_BIT1) +
           (~I2_REVISION_BIT1 * ~REVISION_BIT1)          TO REVISION_BIT1_OK;

ASSIGN     ~DUAL_LINK_OK + (I2_REVISION-BIT2 * REVISION_BIT2) +
           (~I2_REVISION_BIT2 * ~REVISION_BIT2)          TO REVISION_BIT2_OK;

ASSIGN     ~DUAL_LINK_OK + (I2_REVISION_BIT3 * REVISION_BIT3) +
           (~I2_REVISION_BIT3 * ~REVISION_BIT3)          TO REVISION_BIT3_OK;

ASSIGN     ~DUAL_LINK_OK + (I2_REVISION_BIT4 * REVISION_BIT4) +
           (~I2_REVISION_BIT4 * ~REVISION_BIT4)          TO REVISION_BIT4_OK;

ASSIGN     REVISION_BIT1_OK * REVISION_BIT2_OK * REVISION_BIT3_OK *
           REVISION_BIT4_OK                              TO REVISION_NUMBER_OK;

ASSIGN     KILLZ + ~REVISION_NUMBER_OK + CONFIGURE.ERROR      TO KILL;



END LOGIC

NUMERIC BEGIN

//PROGRAM VERIFICATION LOGIC

BLOCK 1 TRIGGERS ON CPS.ENABLE AND STALE AFTER 0:SEC;

//Convert the decimal "REVISION" number to a binary number
//Note_ Additional statements are required should the REVISION number be
greater than 15.
```

```
    IF ((REVISION_NUMBER/1 %  2) =  1) THEN ASSIGN TRUE TO REVISION_BIT1;
END IF
    IF ((REVISION_NUMBER/2 %  2) =  1) THEN ASSIGN TRUE TO REVISION_BIT2;
END IF
    IF ((REVISION_NUMBER/4 %  2) =  1) THEN ASSIGN TRUE TO REVISION_BIT3;
END IF
    IF ((REVISION_NUMBER/8 %  2) =  1) THEN ASSIGN TRUE TO REVISION_BIT4;
END IF


ASSIGN      (ADDRESS_NUMBER <> 10) OR (REVISION_NUMBER <> 13) OR
             (EXECUTIVE_VERSION <> 510)                          TO KILLZ;

END BLOCK

END NUMERIC
```

4.5.15 Logic Queue Overflow

Where too many assign statements have been triggered for execution at one time a Microlok II shutdown may occur due to a logic queue overflow error. This situation may arise at start up when serial links are established and multiple inputs are set at the same time. To overcome this scenario delays may be provided to the establishment of serial links, particularly where multiple serial links are provided.

An example of this application logic is as follows:

```
TIMER BITS

ADJUSTABLE   VSL1JR: SET=40:SEC      CLEAR=0:SEC;
ADJUSTABLE   VSL4JR: SET=20:SEC      CLEAR=0:SEC;

ASSIGN ~CPS.STATUS + ~VSL1JR              TO COMM1.DISABLE; //VITAL LINK
ASSIGN ~CPS.STATUS + ~VSL1JR              TO COMM2.DISABLE; //VITAL LINK
ASSIGN ~VSL4JR                            TO COMM4.DISABLE; //NON-VITAL LINK

ASSIGN CPS.ENABLE + VSL1JR                TO VSL1JR;
ASSIGN CPS.ENABLE + VSL4JR                TO VSL4JR;
```

Input from slaves may be staggered by applying different timers to the address verification bits:

```
ADJUSTABLE       SP25_ADDRESS:   SET=500:MSEC        CLEAR=0:SEC;
ADJUSTABLE       SP23_ADDRESS:   SET=1000:MSEC       CLEAR=0:SEC;
ADJUSTABLE       SP5_ADDRESS:    SET=1500:MSEC       CLEAR=0:SEC;
```

A similar situation may occur when one side fails, resulting in all bits received by the healthly master on the dual link dropping out simultaneously. To overcome this, the up signal control bits received on the dual link for output comparison are made 0.5 seconds slower to drop than other output comparison bits.

All bits received for output comparison are already made slow to drop to ensure that the B_BYPASS bit can pick before the comparisons fail. This is addressed in the Dual Hot Standby Arrangements in Appendix B.

```
B33M_HR:           SET=0:SEC    CLEAR=2000:MSEC;
B33S_HR:           SET=0:SEC    CLEAR=2000:MSEC;
B38MA_HR:          SET=0:SEC    CLEAR=2500:MSEC;
B38SA_HR:          SET=0:SEC    CLEAR=2500:MSEC;
B38MB_HR:          SET=0:SEC    CLEAR=2500:MSEC;
B38SB_HR:          SET=0:SEC    CLEAR=2500:MSEC;
```

4.5.16 Lamp Driven Signals

This section has been left intentionally blank.

4.5.17 Coded Track Circuits

This section has been left intentionally blank

4.5.18 Vital Blocking

This section has been left intentionally blank.

4.5.19 Level Crossings

This section has been left intentionally blank.

4.5.20 Tracks

In general all track inputs are to be provided with a slow to pick timing function.

By the application of a consistent time delay to track circuit operation, there is protection against track bobbing prematurely releasing the interlocking. In CBI interlockings it becomes much easier to be able to provide time delays which present a more consistent time sequence of track circuit operation to the interlocking.

The concept is that by the time a track circuit clear indication is given to the interlocking, a consistent 3 second delay will have been universally applied.

As some track circuits are inherently slow to operate, the CBI input delays may be varied to complement these times and achieve a consistent 3 seconds.

The following table provides details of the inherent slow to pick functionality in the track circuit equipment and the consequential input delay to be applied in the CBI:

Track Circuit Type	Track Circuit Inherent Delay	CBI Input Delay
DC	0	3
AC	0	3
Jeumont	0	3
CSEE	2	1
CSEE DPU	2	1
ML	2	1
Westinghouse FS2500	1.6	1.4
Westinghouse DPU	1.6	1.4
Westinghouse FS2600	1	2
TD4	0	3

4.5.21 Train Stops

The Train Stop normal and reverse detection is brought into the interlocking as direct inputs, hence there are no external VNR and VRR relays. It is essential therefore that the output HR relay function must include the boolean bit VRR and the signal operating circuit is to have the VRR contact replaced with the 'A' track circuit. (Refer to the typical circuits in the appendix)

Note that the Train Stop detection inputs must be crossed proved.

An example of the typical application logic for train stops is as follows:

```
//=================================================================3 TRAINSTOP

ASSIGN      (3VNR + 3M_HR + 3VCSR) * 3AT              TO      3VCSR;

ASSIGN      3M_HR * 3AT                               TO      3VR;

ASSIGN      3VNP * ~3VRP                              TO      3VNR;

ASSIGN      ~3VNP * 3VRP                              TO      3VRR;

ASSIGN      3MHR * 3VRR                               TO      3MHR_OUTPUT;
```

4.5.22 Signals

TZR, SR, and NR

In an OCS interlocking, a new form of TZR function is used as part of the drop-track release of approach locking:

```
ASSIGN      ~3SA_RSR * ~3SB_RSR *
            (~3AT * ((~3BT * 101_NLR) + (3XT * 101_RLR))
            3_TZR * ((~3BT * 101_NLR) + (~3XT * 101_RLR)))          TO 3_TZR;
```

This TZR is provided to minimise the risk of undesired release of approach locking simultaneously with route normalisation under certain failure scenarios.

The SR and NR functions are not required where the application logic is designed with an RSR function as per OCS type interlockings.

In NX style interlockings these functions are as per typical relay circuits as shown following:

```
ASSIGN      ~3AT * (~1CT + 3_TZR)                                   TO 3_TZR;

ASSIGN      48AT * (3M_NLR * 3S_NLR + 3_NR + 3_SR)                  TO 3_SR;

ASSIGN      3_UNR + (~3M_NLR + ~3S_NLR) * ~3M_RSR * ~3S_RSR * 3_NR +
            3_TZR * 1CT * 3_ALSR                                    TO 3_NR;
```

RSR

The RSR function is as per typical OCS type interlockings and ensures the auto normalisation of the signal route through the occupation of the ‘A’ track past the signal.

Where the application is not to be designed as per OCS type interlockings the RSR bit is to be included in series with the UJZR in the stick path of the RUR function.

RUZR

The RUZR function proves the required opposing locking is normal and that all necessary points are locked in the required position or free to be moved. This function is provided as an interlocking safeguard, which continuously monitors the status of the locking. This function has been created for use in the UJZR and RUR functions and avoids the need to duplicate the information.

This bit is also provided to the Control System as a route availability bit.

UJZR

The UJZR function may be referred to as a route free to set expression. This function is required as part of the logic for simulation of the magnetically latched NLR relay.

Note that the UJZR function is given a slow to drop (clear) timing function of 1 second to ensure the RUR will have time to become true and stick up before the UJZR drops.

NLR

The NLR function is held true unless the route is free to set. (via the UJZR) As per typical relay circuits the NLR function is utilised to prove the signal is normal and when down will not become true unless the signal is normal and free of approach locking.

RUR

The RUR function will become true through the route setting control bit (RSR) being set and with the route proven to be free to set via the UJZR bit.

Note the stick path around the UJZR bit.

HR

The HR function is typically an output bit.

For main line routes the HR function will require an intermediate function where train stops are provided. The output HR relay function is to include this intermediate function and the train stop VRR input bit.

ALSR / ALSJR

The ALSR function is as per standard relay circuits with the exception of two timing release paths. The main and shunt routes may have separate ALSJR timing functions as specified in the control tables.

Where the application is designed in line with OCS type interlocking the two-drop-track release path is not to be provided, as a single failure could both drop the RSR and release the approach locking. A new release path based on the new TZR function is used instead.

If a POJR is required to be provided in any ALSR release path then a power off (POR) vital input will be required and assigned to a POJR timing function of 30 seconds slow to set.

Following is an example of typical application logic for a signal and one of the signal routes. Those functions shown that were not previously covered above are designed as per typical relay circuit standards.

Where the Microlok II configuration requires a Hot Standby arrangement reference should also be made to the 'Dual Hot Standby Arrangements' document found in the appendix.

```
//=====================================================================3 SIGNAL


ASSIGN      ~3M_UCR * ~3S_UCR * 3VNR * ~3M_HR * ~3S_HR * 3NGP          TO 3_NGPR;

ASSIGN      3MHP + 3SHP                                                  TO 3RGK;

ASSIGN      3_NGPR * (3_ALSR + ((3M_ALSJR + 3M_NLR) * 3S_ALSJR) +
            (~3AT * 3M_NLR * POJR) +
            (((260.3CT + 1_ALSR) * 1AT) + 3M_NLR) * 1BT * 1CT)          TO 3_ALSR;

ASSIGN      3_NGPR                                                 TO 3M_ALSJR; //120"

ASSIGN      3_NGPR                                                  TO 3S_ALSJR; //60"


//=====================================================================3(M) ROUTE


ASSIGN      ~3_UNR * (3M_URR + (3AT * ~3M_NLR * 3M_RSR))                TO 3M_RSR;

ASSIGN      (3_ALSR + 3M_NLR) *
            ((3AT + 102_RWKR) * 3BT * 3CT +
            3M_USR + 3CTJR + 3BCTJR)                                    TO 3M_USR;

ASSIGN      (3_ALSR + 3M_NLR) * (~3M_RSR + ~3M_UJZR * 3M_NLR) * ~3M_RUR
                                                                        TO 3M_NLR;

ASSIGN      3S_NLR * 6SB_NLR *        ((16M_NLR * 16M_USR) + 103_NLR + 103_WJZR) *
            (101_NLR + 101_WJZR)                                       TO 3M_RUZR;

ASSIGN      3M_RUZR * 3M_RSR * ~3M_NLR * (3M_UJZR + 3M_RUR)             TO 3M_RUR;

ASSIGN      3M_RUZR * ~3A_RSR                                          TO 3M_UJZR;

ASSIGN      3AT * 3BT * 3CT * 9AT * (9BT + 103_RWKR) *
            101_NLKPR * (103_NWKR + (16M_USR * 14AT)) * 3M_RUR          TO 3M_UCR;

ASSIGN      ~3M_USR * ~3CTJR * 9A_VCSR *
            ~3_NGPR * ~3_ALSR * ~3M_ALSJR * 3M_UCR                       TO 3M_HR;

ASSIGN      3M_HR * 3M_HP * 9A_HP * 9VRR                                TO 3M_HDR;

ASSIGN      3M_HDR * 3M_HDP * (9A_HDP + 9A_DP)                          TO 3MA_DR;

// ------------------------------------------------------------------------------------------------------------------
```

4.5.23 Points

The point setting and point locking functions are separate in the application logic design.

The point setting functions NZ and RZ include all the setting conditions to call the points normal or reverse respectively, including the direct point 'key' calls.

WJZR

The WJZR function is provided as an interlocking safeguard, which continuously monitors the status of either the normal or reverse locking depending which way the points are currently laying and the local tracks clear.

The WJZR function can be regarded as a point free to move function.

Note the WJZR is to have a slow to clear timing function of 500 ms and a slow to set timing function of 1 second.

WLZSR

The WLZSR function provides a one shot feature during the initial start up period of the interlocking to allow the point lock relays to initialise in line with the point detection. Until the point lock relays have been initialised it is not possible to drive the points.

The WLZSR function would be down at start up and then permanently true once either of the point locking functions have been established.

To cover the situation where no detection is present during start up the WLZSR is used in the WJZR function to call the points normal in conjunction with the points NR control bit. (Which would need to be true). If the points were lying reverse they would drive normal.

When a point call is not usually present such as in an automatic crossing loop, or push button operated points, the NLR function would also need to be modified. (~WLZSR * ~ RKR would be required to qualify the NZ bit in the points NLR function)

WCZJR

In circumstances other than start up where both the points NLR and RLR functions may be down the WCZJR function is used to set either the NLR or RLR function in line with the detection.

Note that the WCZJR is to have a slow to set timing function of 15 seconds.

NLR / RLR

In conjunction with the points WJZR function the NLR and RLR functions simulate the operation of the magnetically latched relay. The points will remain locked, holding up the NLR or RLR unless the points WJZR function is true.

When a point call is made, via the points NZ or RZ control bit and the points are free to move, the points NLR or RLR function will become true allowing the points to move.

POINTS CONTROL

The following description applies to electrically operated points. EP points will utilise EOL push buttons and require modified data functions.

Points are controlled using three output bits to drive three relays. These output bits and relays are designated NWR, RWR and IR.

If the points NLR function is true then the output bit NWR will call the points normal subject to any further control conditions applied via the IR.

If the points RLR function is true then the output bit RWR will call the points normal subject to any further control conditions applied via the IR.

The isolating relay (IR) function is used to provide an independent over lock on the points by electrically isolating them and also incorporates the points transit function WTJR.

The energisation of the IR enables the points to operate to the position required via either the NWR or RWR being energised.

If the points have not operated and reached the required position within 10 seconds of the IR energising then the WTJR function will become true and the external IR will drop cutting power

to the points.The WTJR is not to time unless conditions permit the IR to be energised. Occupation of local track circuits or operation of the EOL are to reset the WTJR.

The WTJR is to have an adjustable slow to set timing function of 10 seconds.

A separate input into the Microlok II is to be provided for the ESML / EOL. If at any time the handle is removed then the IR will be de-energised cutting power to the points. Loss of the ESML / EOL input will also cause loss of detection. (NWKR and RWKR)

The external IR relays are down proved as inputs into the Microlok II cardfile. Loss of this input will cause a loss of detection. (NWKR and RWKR)

Points are detected using two input bits to provide the primary detection functions. These input bits are designated NKR and RKR and are to be provided separately for each end of a set of points. They are associated with the points control logic in addition to driving the secondary detection.

The NKR and RKR input functions are to be crossed proved in each other.

Two secondary detection functions are to be provided and are designated NWKR and RWKR and are used for interlocking logic conditions in which the WJZR is not required to be down.

Two further detection and locking functions are to be provided and are designated NLKPR and RLKPR and these are used for interlocking logic conditions in which the WJZR is required true.

Following is an example of typical application logic for a set of points. Those functions shown that were not previously covered above are designed as per typical relay circuit standards.

Where the Microlok II configuration requires a Hot Standby arrangement reference should also be made to the 'Dual Hot Standby Arrangements' document found in the appendix.

```
//=================================================================101 POINTS

ASSIGN      ((1M_RUR + 3M_RUR + 3S_RUR + 6SB_RUR) *
            101_CZ + 101_NR) * ~101_RZ                              TO 101_NZ;

ASSIGN      ((6MA_RUR + 6SA_RUR) * 101_CZ + 101_RR) * ~101_NZ       TO 101_RZ;

ASSIGN      101_CR                                                  TO 101_CZ;

ASSIGN      3AT * 8AT *
            ((1M_NLR * 1M_USR * 3M_NLR * 3S_NLR * 6SB_NLR *
            (14MB_USR2 + 8BT) * 101_NLR * ~101_RR) +
            (6MA_NLR * 6SA_NLR *
            (14MB_USR2 + 1CT) *
            (101_RLR * ~101_NR + ~101_WLZSR))) * 101_CZ         TO 101_WJZR;//1"

ASSIGN      (101_NLR + 101_RLR + 101_WLZSR)                     TO 101_WLZSR;

ASSIGN      101_WLZSR * ~101_NLR * ~101_RLR * 101_CZ            TO 101_WCZJR;//15"

ASSIGN      (101_NZ * 101_WJZR + 101_NLR) * ~101_RLR *
            (~101_RZ + ~101_WJZR * 101_NLR) +
            (~101_WLZSR + 101_WCZJR) * 101_NKR * ~101_RKR *
            ~101_RLR * ~101_NLR                                 TO 101_NLR;

ASSIGN      (101_RZ * 101_WJZR + 101_RLR) * ~101_NLR *
            (~101_NZ + ~101_WJZR * 101_RLR) +
            (~101_WLZSR + 101_WCZJR) * 101_RKR * ~101_NKR *
            ~101_NLR * ~101_RLR                                 TO 101_RLR;

ASSIGN      101_NLR                                             TO 101_NWR;

ASSIGN      101_RLR                                             TO 101_RWR;

ASSIGN      101A_NK * 101B_NK * ~101A_RK * ~101B_RK             TO 101_NKR;

ASSIGN      101A_RK * 101B_RK * ~101A_NK * ~101B_NK             TO 101_RKR;
```

```
ASSIGN      (101_NLR * ~101_NKR + 101_RLR * ~101_RKR) *
            ~101_WTJR * 101_EOL *
            (6_ALSR * 3AT * 8AT + 101_IR)                          TO 101_IR;

ASSIGN      (101_NWR * ~101_NKR + 101_RWR * ~101_RKR) *
            101_EOL                                                TO 101_WTJR;//10"

ASSIGN      ~101_WJZR * 101_NWKR * ~101_RLKPR                      TO 101_NLKPR;

ASSIGN      ~101_WJZR * 101_RWKR * ~101_NLKPR                      TO 101_RLKPR;

ASSIGN      101_NKR * 101_NLR * ~101_RKR * ~101_IR * 101_IZ *
            101_EOL                                                TO 101_NWKR;

ASSIGN      101_RKR * 101_RLR * ~101_NKR * ~101_IR * 101_IZ *
            101_EOL                                                TO 101_RWKR;
// ------------------------------------------------------------------------------------------------------------
```

4.5.24 Ground Frames

An example of the typical application logic for ground frames is as follows:

```
//================================================================= FRAME D - 20 /

ASSIGN      19_WJZR * (20_NR + 20_SR)                              TO 20_SR;

ASSIGN      3SB_NLR * (46M_NLR + 20_RLR) * (19_RLR + 19_WJZR * 20_SR)
                                                                   TO 20_RWZR;

ASSIGN      20_RWZR * ~20RR                                        TO 20_WJZR;

ASSIGN      (~20RR + ~20_WJZR * 20_NLR) * ~20_RLR * 3SA_NLR *
            (20NR * 20_NR + 20_NLR)                                TO 20_NLR;

ASSIGN      20RR * (20_WJZR + 20_RLR) *
            20_RWZR * ~20NR * ~20_NLR                              TO 20_RLR;

ASSIGN      20_RLR * ~20_NR * 19_RWKR                              TO RELSW_D_REV;

ASSIGN      20_NZR                                                 TO 20_NKR;

ASSIGN      20_RZR                                                 TO 20_RKR;

ASSIGN      20_NKR * ~20_RLR * ~RELSW_D_REV *
            RELSW_D_CZR * ~4_FR_D_LPR * FR_D_EM_REP                TO 20_NR;

ASSIGN      20_RKR * 20_RLR * RELSW_D_REV * ~RELSW_D_CZR           TO 20_RR;
// ------------------------------------------------------------------------------------------------------------
```

5. Circuit Design

5.1. Microlok II Design Configuration and Settings

In order to provide consistency between applications the following guidelines are to be followed by designers. In many cases, the items are not absolutes, and if a preferable arrangement is proposed for a specific job, the ARTC General Manager ISP or nominated Signalling representative may give approval.

5.1.1 Arrangements of Cards in Card Files

Previous installations installed the CPU and Power Supply in the left most position of the card file. There may be advantages in installing these boards on the right hand side. Where the card file is likely to be filled to capacity, installation on the right hand side may be preferable. However where card files are considered for the installation of split card files, this may cause difficulty.

From the left hand side, other cards should be installed as follows:

CPU
Power Supplies
Coded Track Circuit Cards
Lamp Drivers
Vital Outputs
Vital Inputs
NV I/0 Cards
Code Interface Cards

5.1.2 Microlok II Power Consumption

Microlok Tools version 5 has a power calculator as one of the tools. This allows you to assess the power consumption on each of the Microlok internal power supplies based on your design configuration.

The calculator assumes the worst case, so you may have to 'discount' and make allowance for the specifics of the particular arrangement. For example, most signalling inputs have a normal and a reverse for a function. Only one can be on at a time and consequently this can result in the power consumption being less than indicated. However remember that tracks can all be up together so you cannot usually just halve the figures.

Also, the calculator in version 5 is based on power supply cards which have now been superseded. The latest power supply card has higher current capacities: 5 amps on the +5V supply, and 2 amps on the -12V supply. The +12V supply is unchanged at 1 amp.

When the power consumption is beyond that which can be handled by the Power Supply card, it becomes necessary to provide an external power supply.

The power supply card also provides for the connection of the VCOR relay and the 250Hz CPS signal to the CPU.

No VCOR Required

If the cardfile is being used in a situation where no VCOR relay is required (i.e. CPU only, or CPU and input cards only) then the power supply card is not provided, and the external power supply unit is connected to the Microlok by means of the terminals on the back of the cardfile behind slot 19.

VCOR Required

Where a VCOR is required because the cardfile contains output cards, or lamp driver cards, a CPS card is required.

CPS card N451910-7501. This is a double width card the same as the power supply card. This card provides the connection to the VCOR and also the 250Hz CPS signal to the CPU. When this card is used the external power supply must be connected not only to the back plane terminals

behind slot 19, but also into the CPS card. The wiring for this is shown in the US&S manuals in section 2.1.3.1 of the 6800B manual and page 2-4.

A UPS will usually be needed at the source of the new external supplies.

6. Setting to Work

Experience with setting to work Microlok II systems has shown that many of the faults reoccur and having seen it before, it becomes easy to identify. The following gives a description of those faults and the possible causes:

1. Power is on, but no signs of life.
   - Check the supply voltage. Boot up requires at least 11V to occur reliably.
2. System boots and data is loaded, but the system will not accept the user configuration address and version number.
   - User configurable items are stored in the EEPROM on the CPU plug coupler. Check that the wiring from the EEPROM is correct and that the crimps are good and pushed well home in the plug.
3. System will not accept version numbers with leading zeros (i.e. 008).
   - Do not use leading zeros in version numbers, they should be straight numeric values (e.g. 1,2,3,4,5,6,7,8,9,10,11 etc).
4. System starts, but LED's on coded track card light, then fade away.
   - There is no power on the coded track card. Check the main 12V supply and negative return to this card and condition of fuses and links
5. System starts but CPS and VCOR do not pick.
   - Ensure the dip switches or jumper pins on the card plugs are correctly set. Ensure all cards are powered where necessary (e.g. Output, lamp drive).
6. VCOR does not pick, but CPS light on the power supply card is on.
   - Check the VCOR negative pin is in, and the relay is wired correctly. Note that the CPS delivers a greater negative than the N12 does, and the relay is biased.
7. System boots, but CPS cycles and VCOR picks and drops until system locks out.
   - Check that the VCOR supply to the cards is present (especially output and lamp driver cards). Check the VCOR fuse, and that the crimps in the plug couplers are correct and pushed fully home. Also check the VCOR has front contacts in use, for the VCOR bus and card supplies.
   - Check the error log using the Microlok Tools to narrow the fault to a specific card.
8. System still having problems and it is hard to isolate the fault.
   - With PC Link, ensure the data for the cards has "Adjustable" Enable rather than "Fixed". Use the Tools programme to turn off (disable) all the cards, and then switch each on progressively.
9. System has had a critical error.
   - Go into the 'Reset' menu then to 'PC Link' mode. Accept this mode and the 'Tools' programme should work ok.
   - Remember to Clear the CPS before attempting to run the system.
10. When a negative pin on a relay output is pulled, the system fails.
    - Multiple output relays may have been looped on the negative side and a common pin used. The Microlok sees both outputs via the 2 relay coils. Each output relay must have its own negative pin.
11. System works ok with signal lamps disconnected, but resets when the lamps are pinned up.
    - The Microlok likes to see the correct lamp current being pulled. Check that the output current to the lamp is at least 1.5A. Currents around 1A can cause problems.

12. What cables do I need to connect things together?
    - The laptop when connected to the CPU diagnostic port, needs a special cable with 9 pin connectors. Details of the cable are in the Microlok manual.
    - Where Citect is connected to a CPU communications port, a Null Modem (crossed) cable is required.
    - Where a modem is connected, a standard RS232 (straight through) cable is required.
13. System runs O.K. and Non-Vital I/O card shows output LED's O.K. but, output relays do not pick up.
    - Ensure adequate negative return wires have been wired out of the card. You will probably need more than the manual specifies. A minimum of four should be provided, and more if a larger number of relays is installed. The number quoted in the manual should be O.K. for LED drives only.

7. Appendix A – Typical Circuits

				30/9/03	13:45		Rev 01	C0220A50	CPU BOARD JUMPER AND DIP SWITCH SETTINGS		SHT: A50	CB: 022

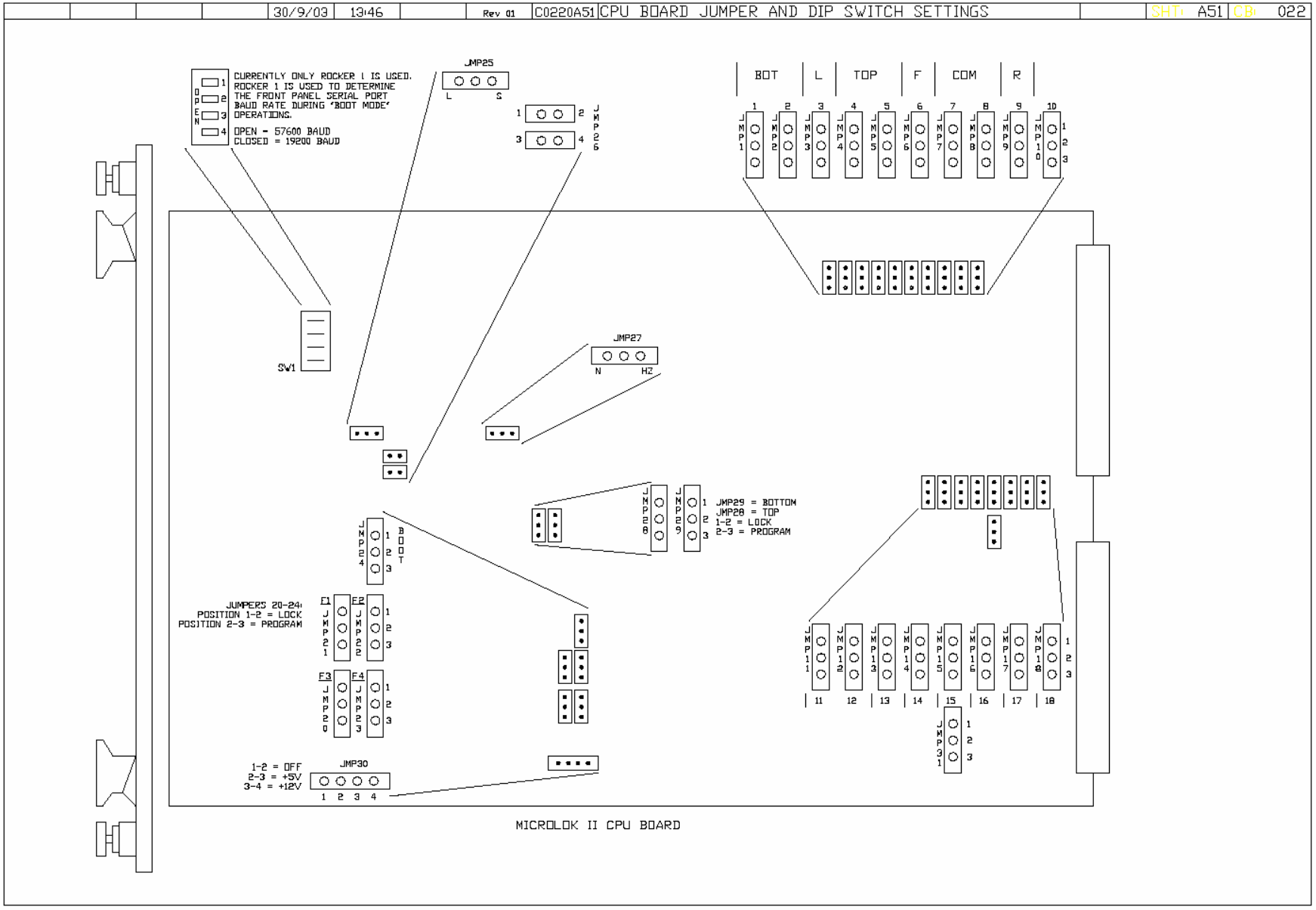
MICROLOK II CPU BOARD JUMPER POSITIONS

JUMPER ID	DESCRIPTION	POSITION	NOTES
JMP1	BOTTOM PCMCIA 2 WAIT STATES	2-3	
JMP2		NOT INSTALLED	
JMP3	ON-BOARD RAM 1 WAIT STATE	2-3	1
JMP4	TOP PCMCIA 2 WAIT STATES	2-3	
JMP5		NOT INSTALLED	
JMP6	FLASH 1 WAIT STATE	2-3	1
JMP7	ENABLE COM4 RXD	1-2	
JMP8	ENABLE COM4 DCD	1-2	
JMP9	DISABLE BACKPLANE CPU RESET	1-2	
JMP10	COM1 TX.CLK IS AN OUTPUT	2-3	
JMP11	COM3 VOLTAGE DRIVE LEVELS RS-232	1-2	
	RS-423	2-3	
JMP12	COM3 VOLTAGE DRIVE LEVELS RS-232	1-2	
	RS-423	2-3	
JMP13	COM3 TX.CLK IS AN OUTPUT	2-3	
JMP14	COM3 TX.CLK IS AN OUTPUT	1-2	
JMP15	COM4 RX.CLK = 9.83Mhz	1-2	
JMP16	COM3 RX.CLK = 9.83Mhz	1-2	
JMP17	COM2 RX.CLK = 9.83Mhz	1-2	
JMP18	COM1 RX.CLK = 9.83Mhz	1-2	
JMP19	NOT AVAILABLE	N/A	
JMP20	FLASH 3 PROGRAMMING LANGUAGE LOCKED	1-2	2
	(APPLICATION SPACE) PROGRAM	2-3	

JUMPER ID	DESCRIPTION	POSITION	NOTES
JMP21	FLASH 1 PROGRAMMING LANGUAGE LOCKED	1-2	2
	(EXECUTIVE SPACE) PROGRAM	2-3	
JMP22	FLASH 2 PROGRAMMING LANGUAGE LOCKED	1-2	2
	(EXECUTIVE SPACE) PROGRAM	2-3	
JMP23	FLASH 4 PROGRAMMING LANGUAGE LOCKED	1-2	2
	(APPLICATION SPACE) PROGRAM	2-3	
JMP24	FLASH 1 BOOT BLOCK LOCKED	1-2	2
	(BOOT SPACE) PROGRAM	2-3	
JMP25	SPEAKER VOLUME SOFT	2-3	
	LOUD	1-2	
	OFF	NOT INSTALLED	
JMP26	IRQ7 OFF	2-4	
JMP27	68332 NORMAL	1-2	1
JMP28	TOP PCMCIA PROGRAMMING VOLTAGE LOCKED	1-2	2
	PROGRAM	2-3	
JMP29	BOTTOM PCMCIA PROGRAMMING VOLTAGE LOCKED	1-2	2
	PROGRAM	2-3	
JMP30	FLASH PROGRAMMING VOLTAGE OFF	1-2	2
	5V	2-3	
	12V	3-4	
JMP31	CPS DRIVE NORMAL	1-2	1

NOTES:

1. IF HEADER POSTS ARE NOT INSTALLED IN THESE LOCATIONS, NO JUMPER IS REQUIRED.
2. SETTINGS SHOWN UNDERLINED ARE THE NORMAL JUMPER POSITIONS, WHICH LOCK THE FLASH DEVICES AND PREVENT THEIR CONTENTS FROM BEING MODIFIED.


30/9/03
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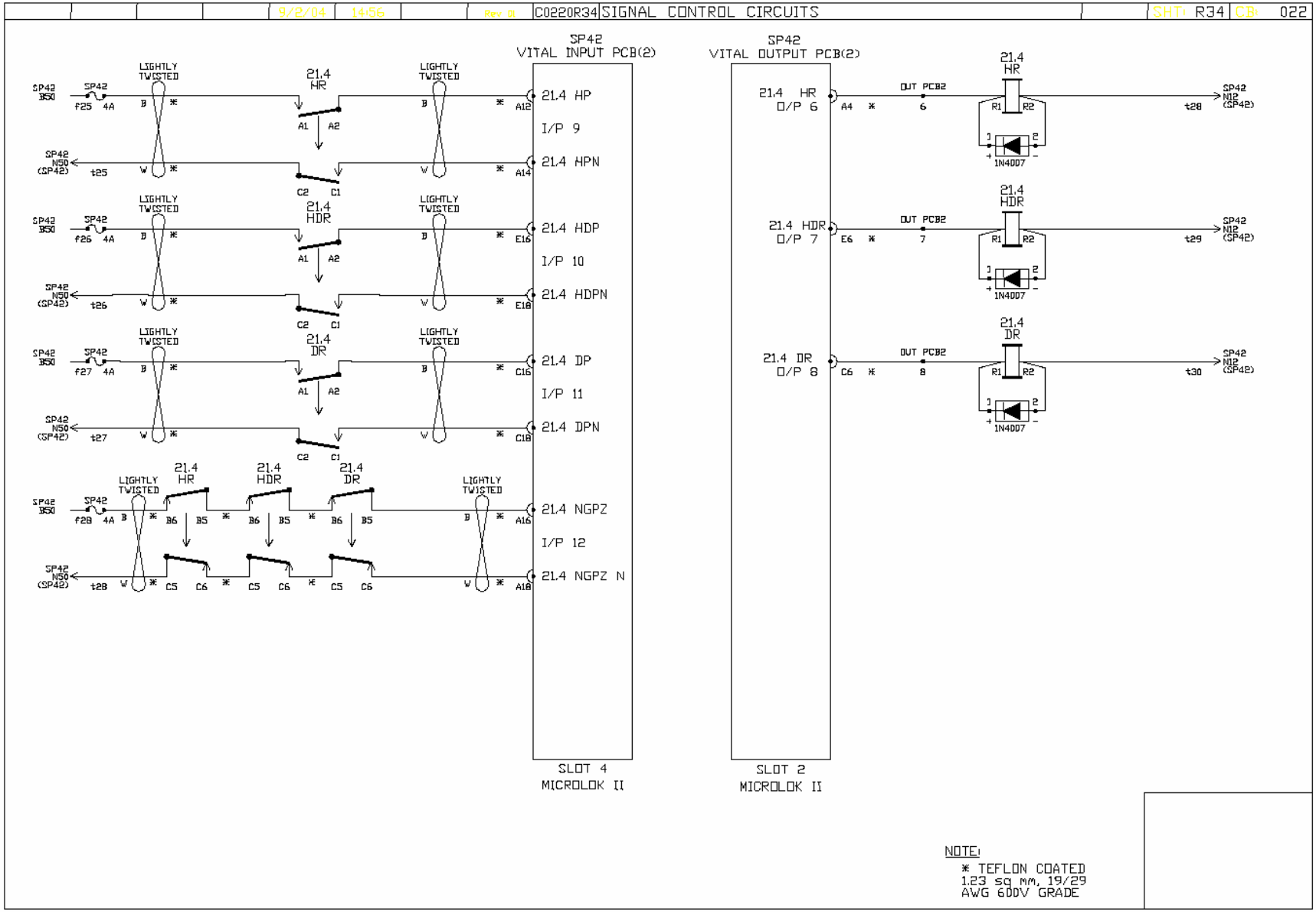
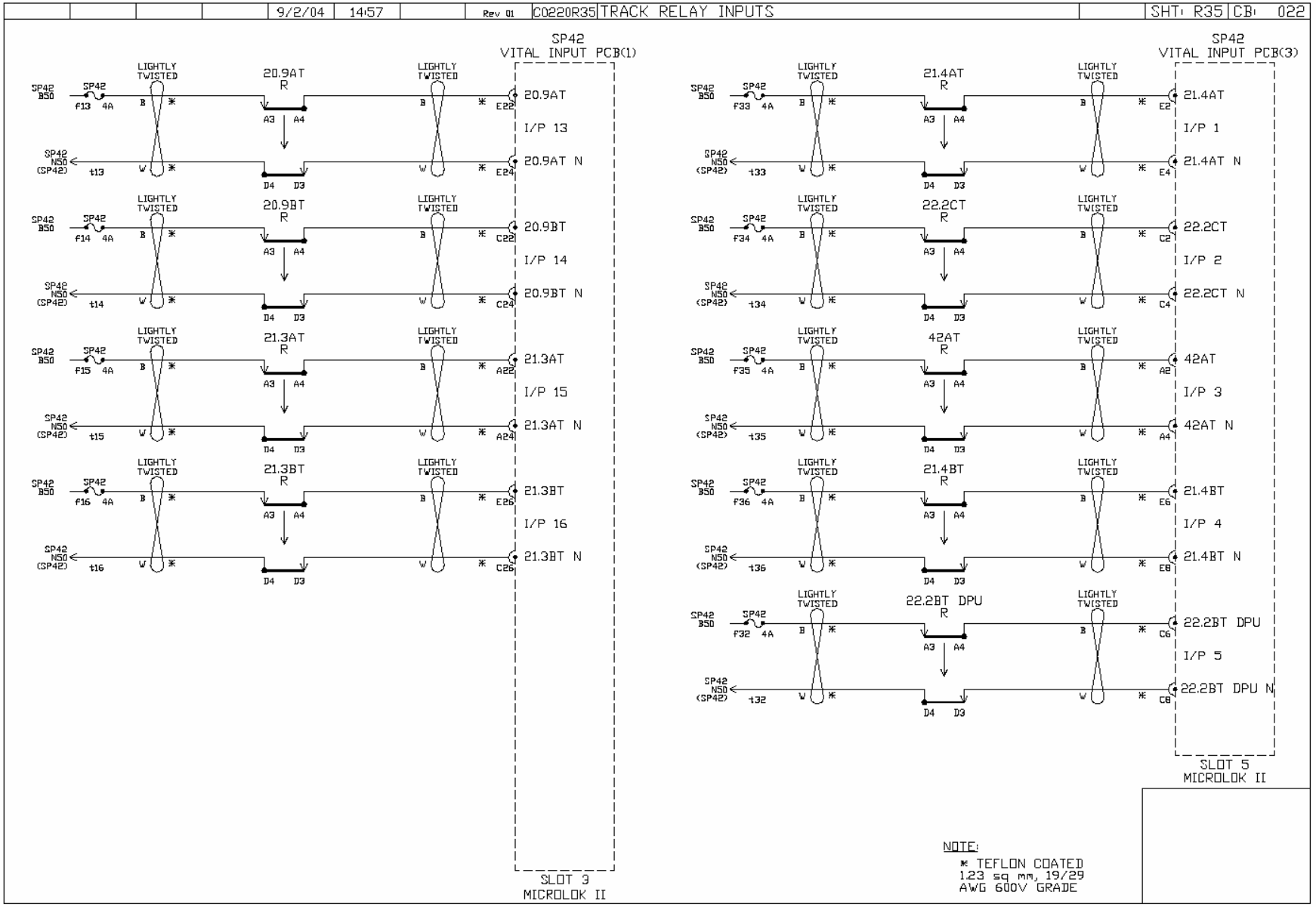
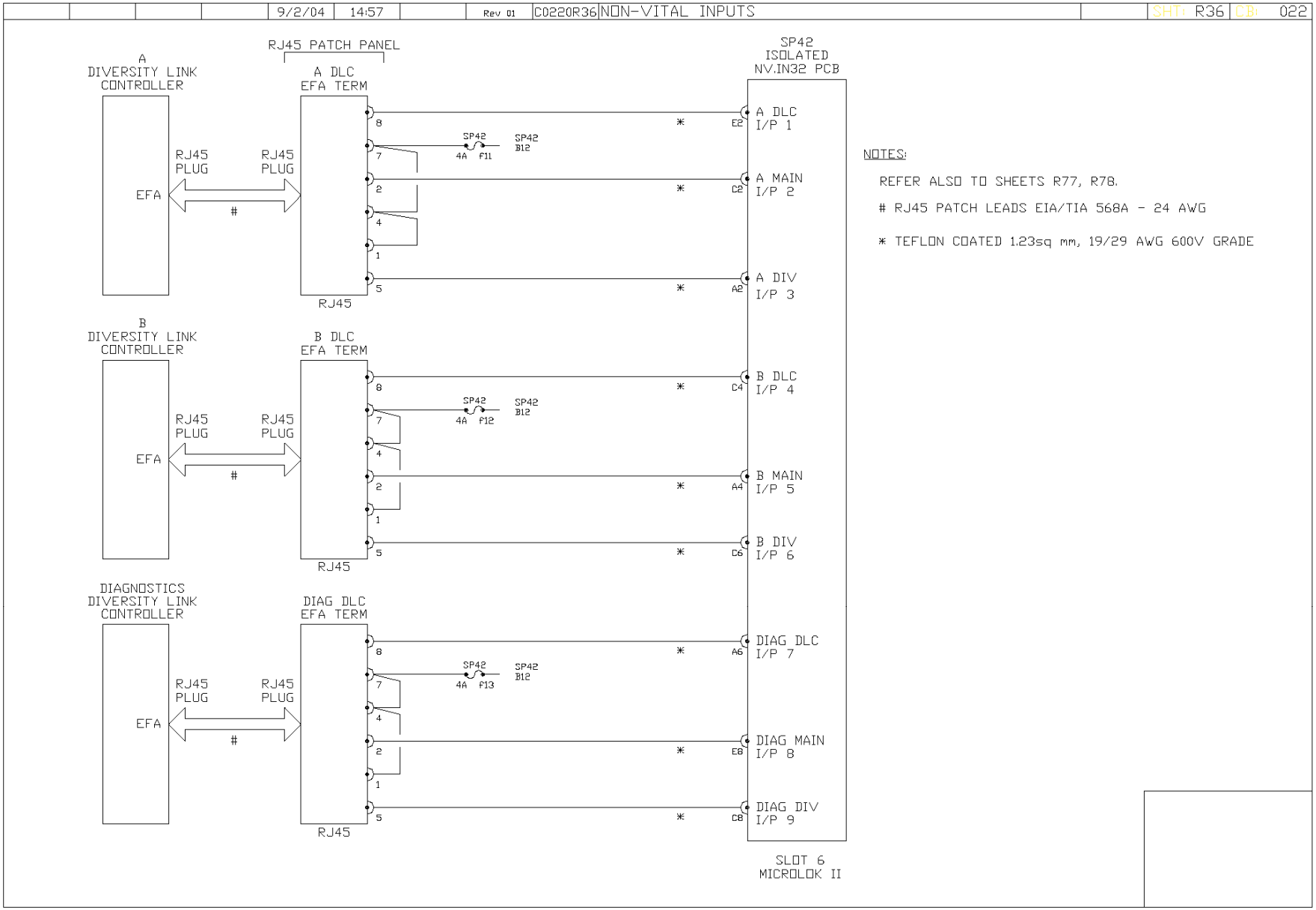
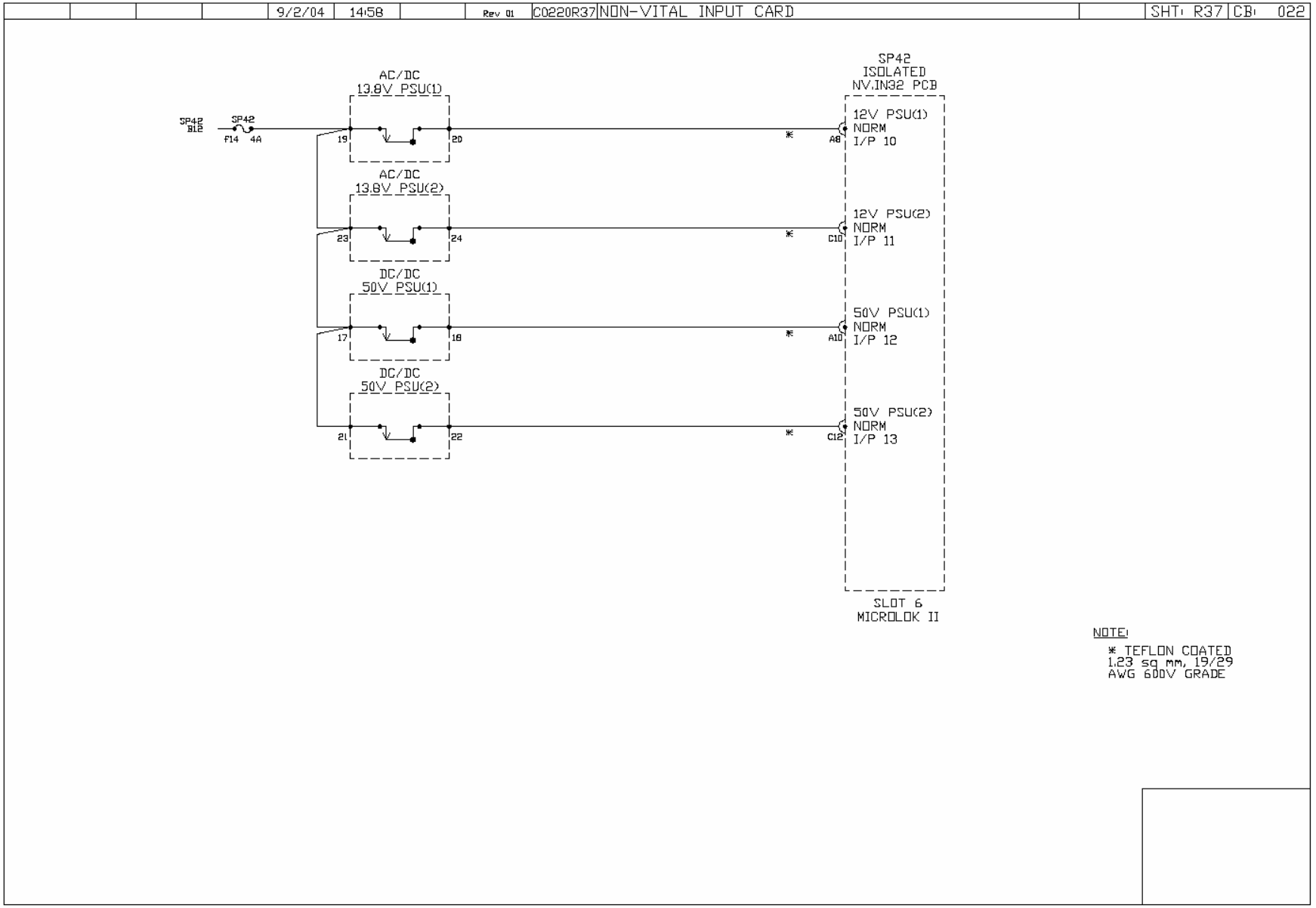
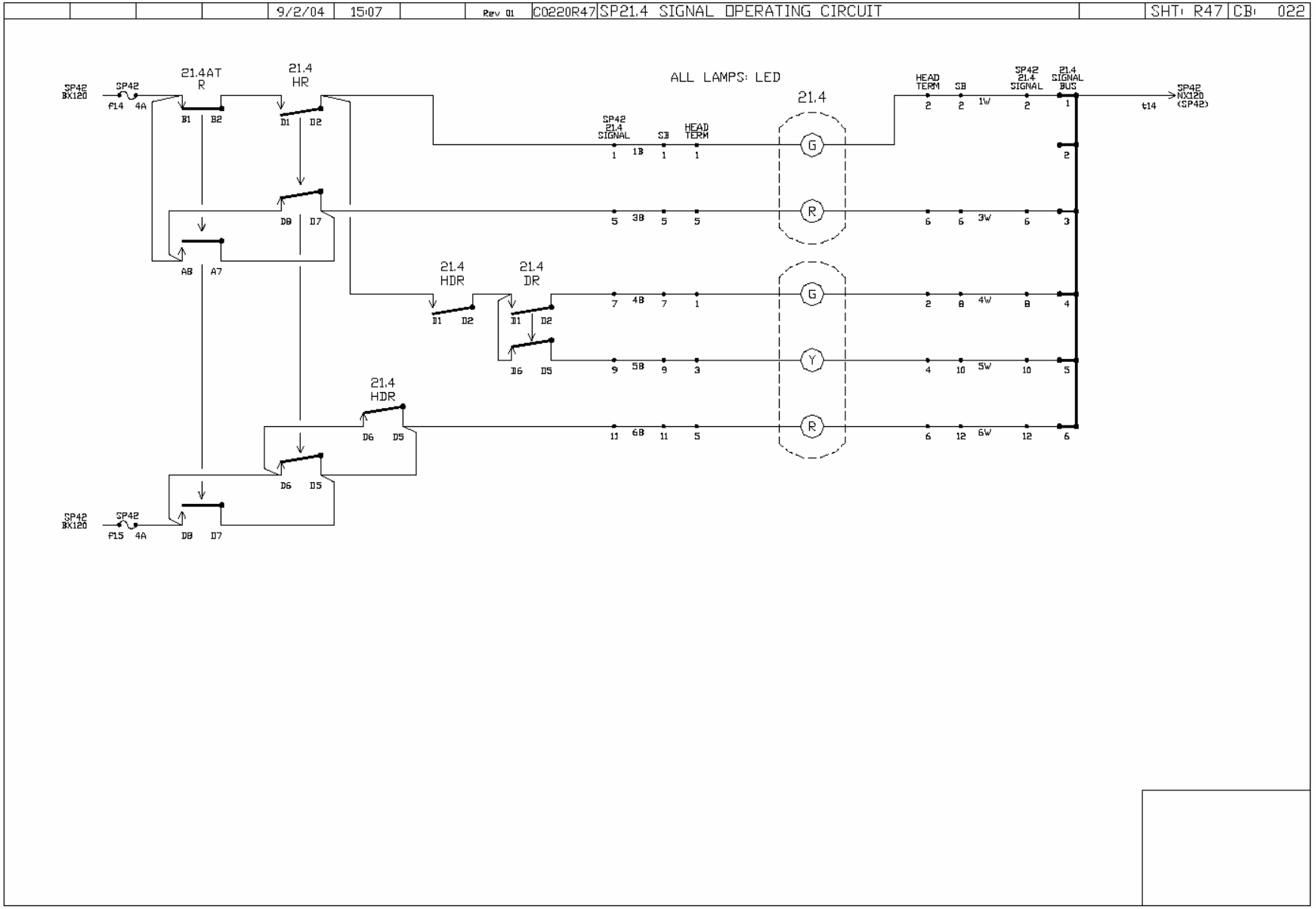
Rev 01
C0220A51
CPU BOARD JUMPER AND DIP SWITCH SETTINGS
SHT: A51
CB: 022
CURRENTLY ONLY ROCKER 1 IS USED.
ROCKER 1 IS USED TO DETERMINE
THE FRONT PANEL SERIAL PORT
BAUD RATE DURING 'BOOT MODE'
OPERATIONS.
OPEN = 57600 BAUD
CLOSED = 19200 BAUD
JMP25
L
S
BOT
L
TOP
F
COM
R
SW1
JMP27
N
HZ
JMP29 = BOTTOM
JMP28 = TOP
1-2 = LOCK
2-3 = PROGRAM
BOOT
JUMPERS 20-24:
POSITION 1-2 = LOCK
POSITION 2-3 = PROGRAM
1-2 = OFF
2-3 = +5V
3-4 = +12V
JMP30
MICROLOK II CPU BOARD

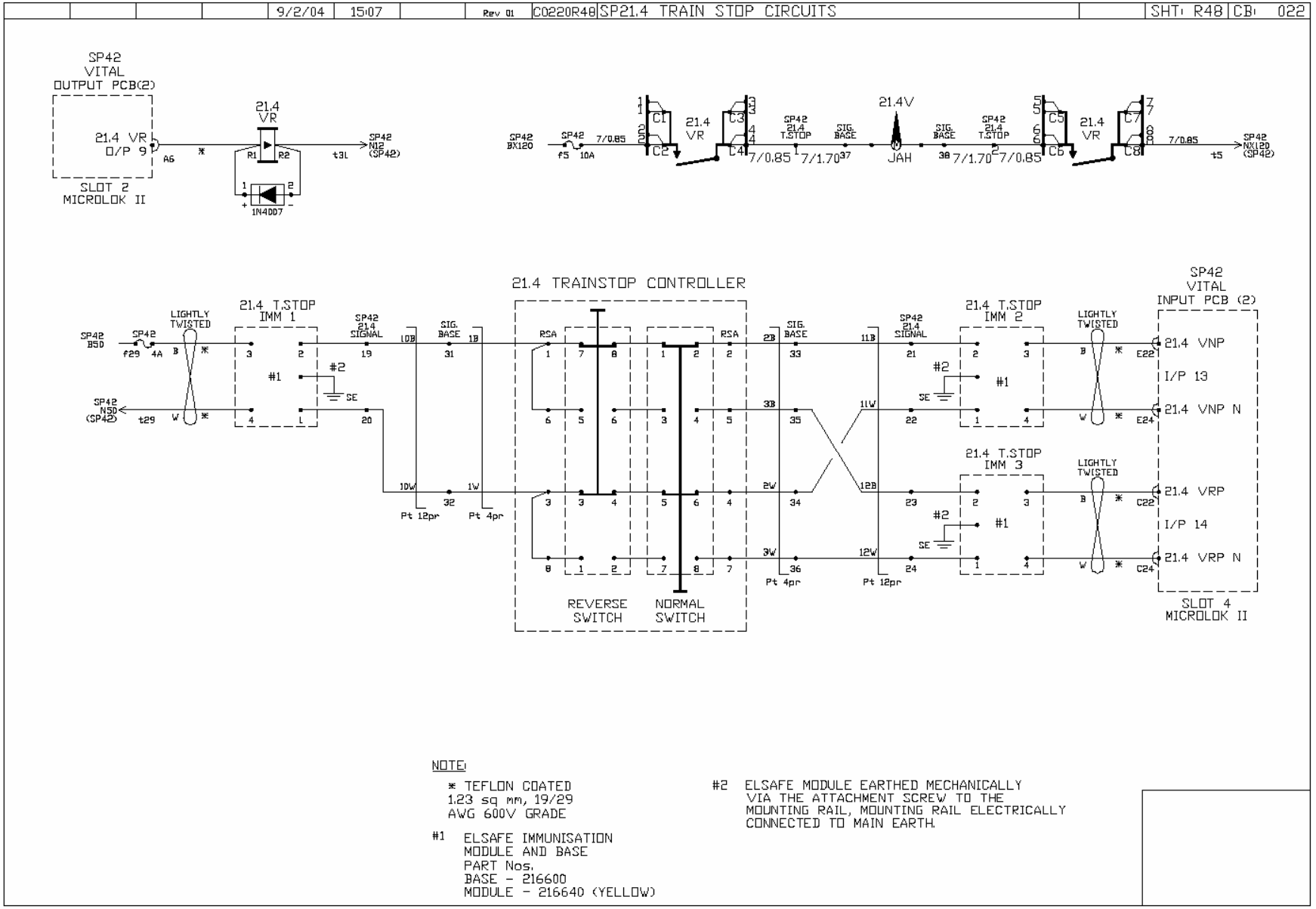

9/2/04
14:56
Rev 01
C0220R34 SIGNAL CONTROL CIRCUITS
SHT: R34
CB: 022
SP42
VITAL INPUT PCB(2)
SP42
VITAL OUTPUT PCB(2)
LIGHTLY TWISTED
21.4 HR
21.4 HDR
21.4 DR
21.4 HP
I/P 9
21.4 HPN
21.4 HDP
I/P 10
21.4 HDPN
21.4 DP
I/P 11
21.4 DPN
21.4 NGPZ
I/P 12
21.4 NGPZ N
21.4 HR O/P 6
21.4 HDR O/P 7
21.4 DR O/P 8
OUT PCB2
1N4007
SLOT 4
MICROLOK II
SLOT 2
MICROLOK II
NOTE:
* TEFLON COATED
1.23 sq mm, 19/29
AWG 600V GRADE


9/2/04 14:57 Rev 01 C0220R35 TRACK RELAY INPUTS SHT: R35 CB: 022
SP42 VITAL INPUT PCB(1)
20.9AT R
20.9AT
I/P 13
20.9AT N
20.9BT R
20.9BT
I/P 14
20.9BT N
21.3AT R
21.3AT
I/P 15
21.3AT N
21.3BT R
21.3BT
I/P 16
21.3BT N
SLOT 3 MICROLOK II
SP42 VITAL INPUT PCB(3)
21.4AT R
21.4AT
I/P 1
21.4AT N
22.2CT R
22.2CT
I/P 2
22.2CT N
42AT R
42AT
I/P 3
42AT N
21.4BT R
21.4BT
I/P 4
21.4BT N
22.2BT DPU R
22.2BT DPU
I/P 5
22.2BT DPU N
SLOT 5 MICROLOK II
LIGHTLY TWISTED
NOTE:
* TEFLON COATED 1.23 sq mm, 19/29 AWG 600V GRADE


9/2/04 14:57 Rev 01 C0220R36 NON-VITAL INPUTS SHT: R36 CB: 022
RJ45 PATCH PANEL
SP42 ISOLATED NV.IN32 PCB
A DIVERSITY LINK CONTROLLER
A DLC EFA TERM
RJ45 PLUG
RJ45 PLUG
EFA
#
RJ45
SP42 4A F11
SP42 B12
A DLC I/P 1
A MAIN I/P 2
A DIV I/P 3
B DIVERSITY LINK CONTROLLER
B DLC EFA TERM
SP42 4A F12
B DLC I/P 4
B MAIN I/P 5
B DIV I/P 6
DIAGNOSTICS DIVERSITY LINK CONTROLLER
DIAG DLC EFA TERM
SP42 4A F13
DIAG DLC I/P 7
DIAG MAIN I/P 8
DIAG DIV I/P 9
SLOT 6 MICROLOK II
NOTES:
REFER ALSO TO SHEETS R77, R78.
RJ45 PATCH LEADS EIA/TIA 568A - 24 AWG
* TEFLON COATED 1.23sq mm, 19/29 AWG 600V GRADE


9/2/04
14:58
Rev 01
C0220R37
NON-VITAL INPUT CARD
SHT: R37
CB: 022
SP42
ISOLATED
NV.IN32 PCB
AC/DC
13.8V PSU(1)
AC/DC
13.8V PSU(2)
DC/DC
50V PSU(1)
DC/DC
50V PSU(2)
SP42
B12
SP42
F14 4A
19
20
23
24
17
18
21
22
A8
C10
A10
C12
12V PSU(1)
NORM
I/P 10
12V PSU(2)
NORM
I/P 11
50V PSU(1)
NORM
I/P 12
50V PSU(2)
NORM
I/P 13
SLOT 6
MICROLOK II
NOTE:
* TEFLON COATED
1.23 sq mm, 19/29
AWG 600V GRADE


9/2/04
15:07
Rev 01
C0220R47
SP21.4 SIGNAL OPERATING CIRCUIT
SHT: R47
CB: 022
ALL LAMPS: LED
21.4
21.4AT R
21.4 HR
21.4 HDR
21.4 DR
21.4 HDR
SP42 BX120
SP42 f14 4A
SP42 f15 4A
SP42 21.4 SIGNAL
SB
HEAD TERM
SP42 21.4 SIGNAL
21.4 SIGNAL BUS
SP42 NX120 (SP42)
G
R
Y


9/2/04
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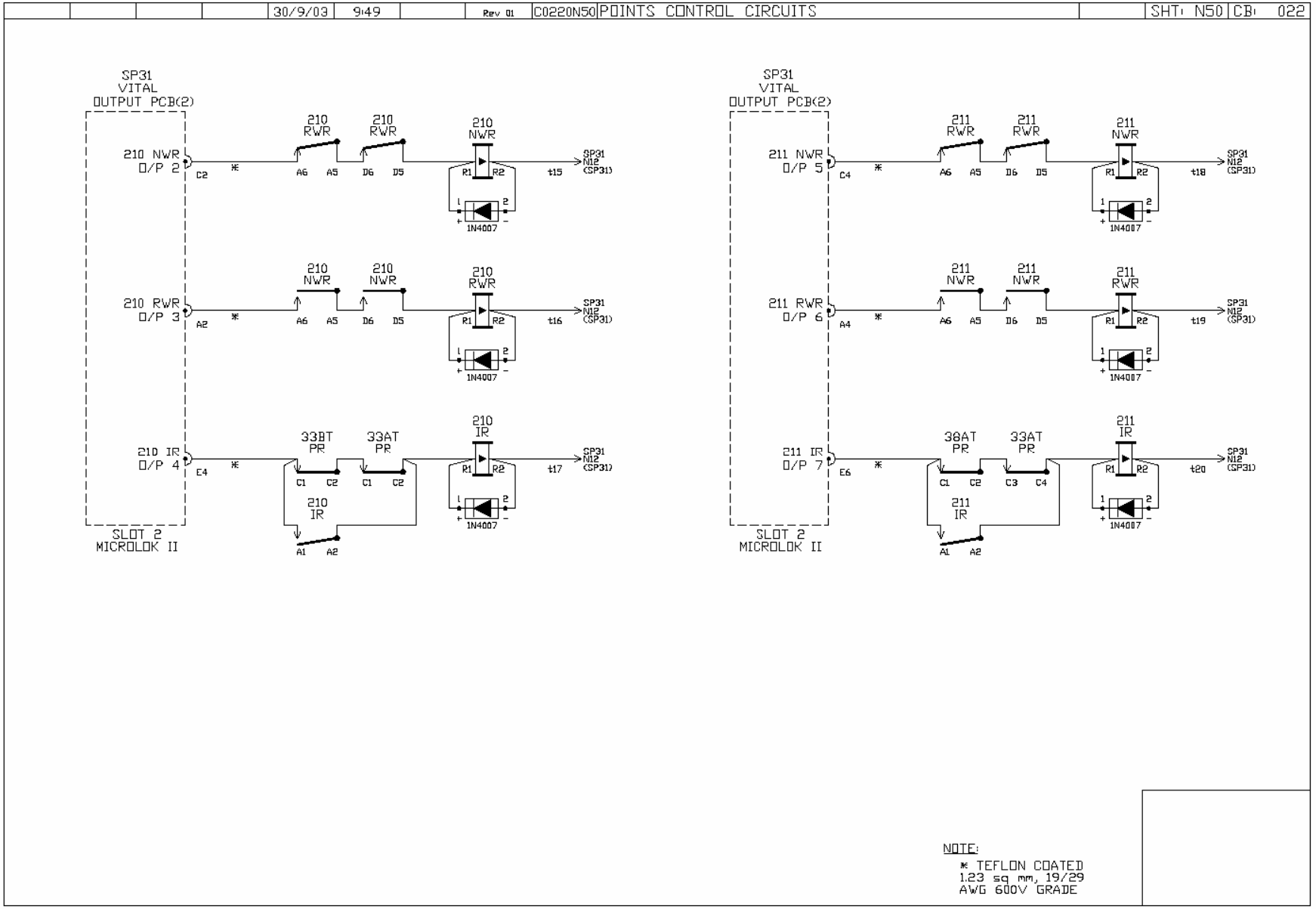
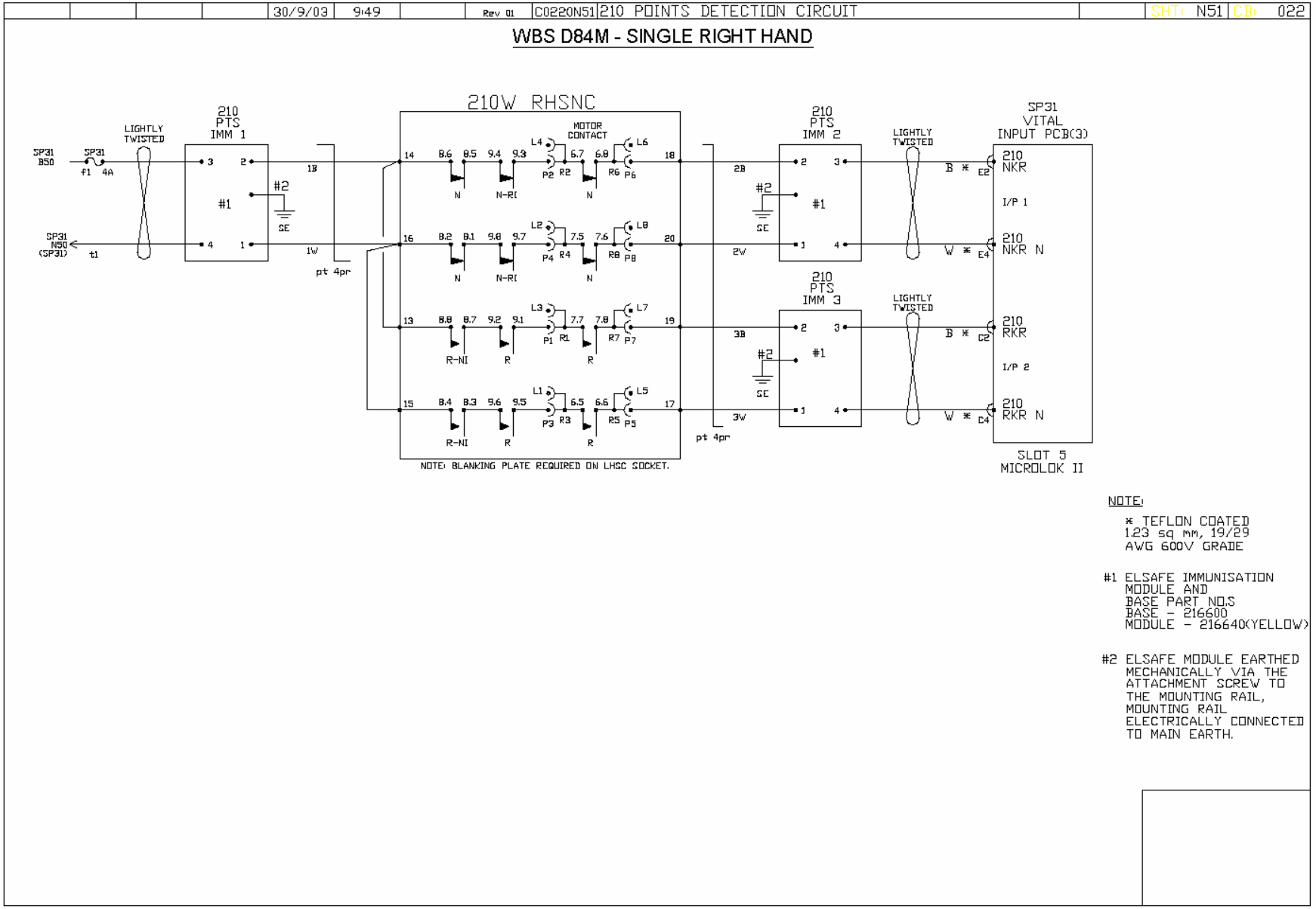
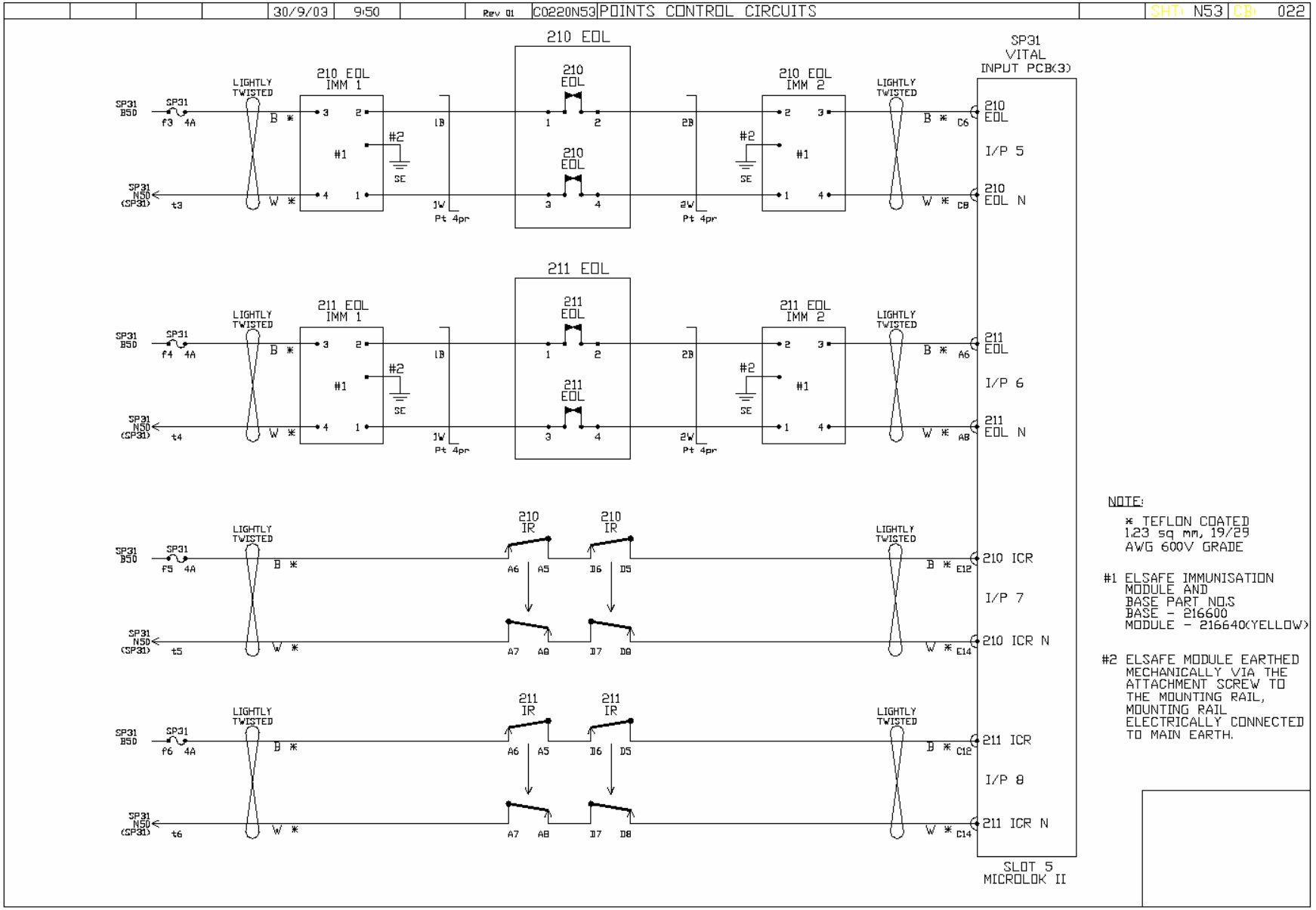
Rev 01
C0220R48
SP21.4 TRAIN STOP CIRCUITS
SHT: R48
CB: 022
SP42
VITAL
OUTPUT PCB(2)
21.4 VR
O/P 9
SLOT 2
MICROLOK II
1N4007
21.4 VR
21.4V
JAH
21.4 TRAINSTOP CONTROLLER
21.4 T.STOP
IMM 1
IMM 2
IMM 3
LIGHTLY TWISTED
SP42
21.4
SIGNAL
SIG.
BASE
RSA
REVERSE
SWITCH
NORMAL
SWITCH
SP42
VITAL
INPUT PCB (2)
21.4 VNP
I/P 13
21.4 VNP N
21.4 VRP
I/P 14
21.4 VRP N
SLOT 4
MICROLOK II
Pt 12pr
Pt 4pr
SE
#1
#2
NOTE:
* TEFLON COATED
1.23 sq mm, 19/29
AWG 600V GRADE
#1 ELSAFE IMMUNISATION
MODULE AND BASE
PART Nos.
BASE - 216600
MODULE - 216640 (YELLOW)
#2 ELSAFE MODULE EARTHED MECHANICALLY
VIA THE ATTACHMENT SCREW TO THE
MOUNTING RAIL, MOUNTING RAIL ELECTRICALLY
CONNECTED TO MAIN EARTH.


30/9/03
9:49
Rev 01
C0220N50
POINTS CONTROL CIRCUITS
SHT: N50
CB: 022
SP31
VITAL
OUTPUT PCB(2)
210 NWR
O/P 2
210 RWR
O/P 3
210 IR
O/P 4
SLOT 2
MICROLOK II
210 RWR
210 RWR
210 NWR
210 NWR
210 NWR
210 RWR
33BT PR
33AT PR
210 IR
210 IR
1N4007
SP31 N12 (SP31)
211 NWR
O/P 5
211 RWR
O/P 6
211 IR
O/P 7
211 RWR
211 RWR
211 NWR
211 NWR
211 NWR
211 RWR
38AT PR
33AT PR
211 IR
211 IR
NOTE:
* TEFLON COATED
1.23 sq mm, 19/29
AWG 600V GRADE


30/9/03
9:49
Rev 01
C0220N51 210 POINTS DETECTION CIRCUIT
SHT: N51
CB: 022
WBS D84M - SINGLE RIGHT HAND
210W RHSNC
MOTOR CONTACT
210 PTS IMM 1
210 PTS IMM 2
210 PTS IMM 3
LIGHTLY TWISTED
SP31 VITAL INPUT PCB(3)
SP31 B50
SP31 N50 (SP31)
210 NKR
I/P 1
210 NKR N
210 RKR
I/P 2
210 RKR N
pt 4pr
NOTE: BLANKING PLATE REQUIRED ON LHSC SOCKET.
SLOT 5 MICROLOK II
NOTE:
* TEFLON COATED 1.23 sq mm, 19/29 AWG 600V GRADE
#1 ELSAFE IMMUNISATION MODULE AND BASE PART NOS BASE - 216600 MODULE - 216640(YELLOW)
#2 ELSAFE MODULE EARTHED MECHANICALLY VIA THE ATTACHMENT SCREW TO THE MOUNTING RAIL, MOUNTING RAIL ELECTRICALLY CONNECTED TO MAIN EARTH.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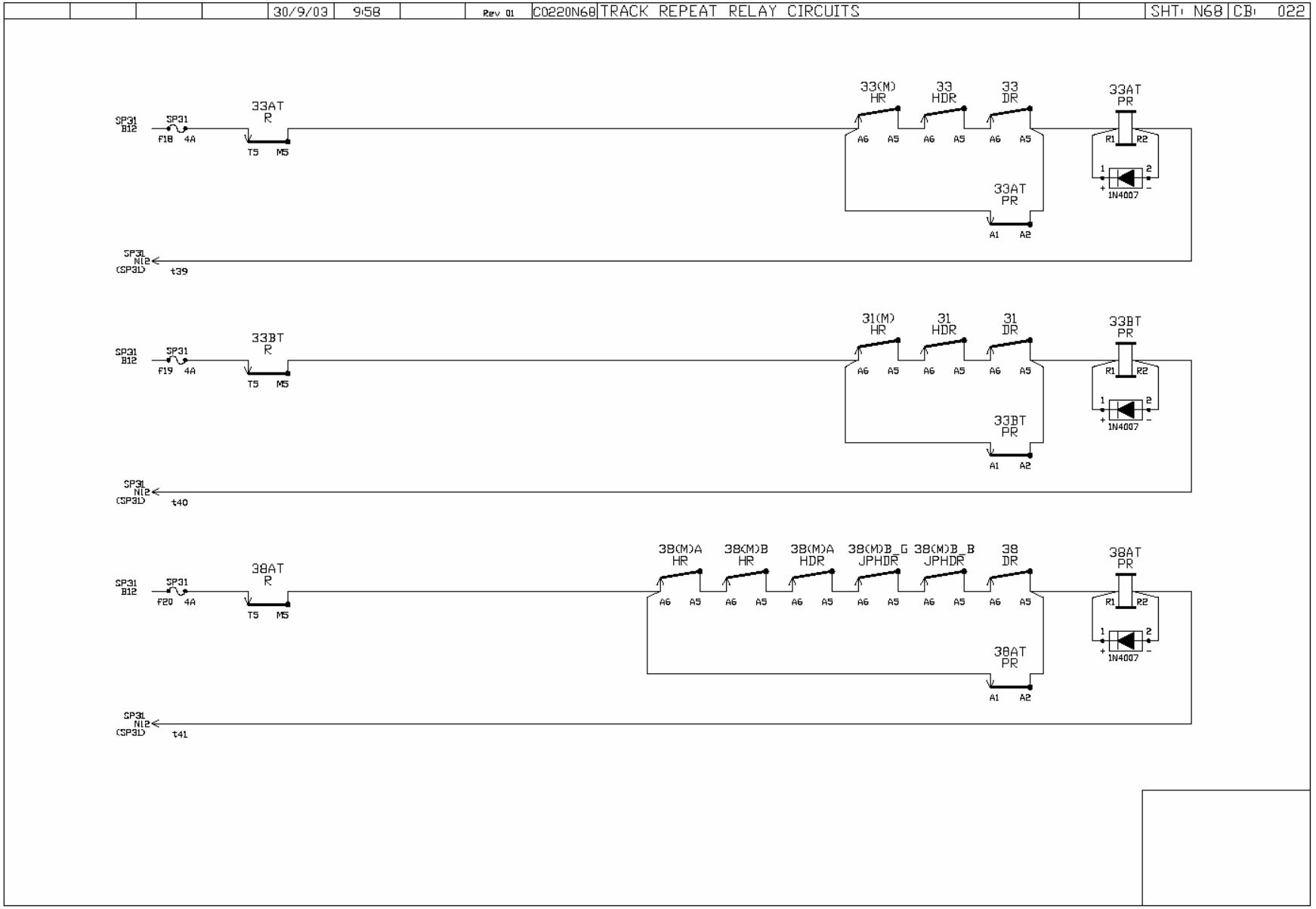
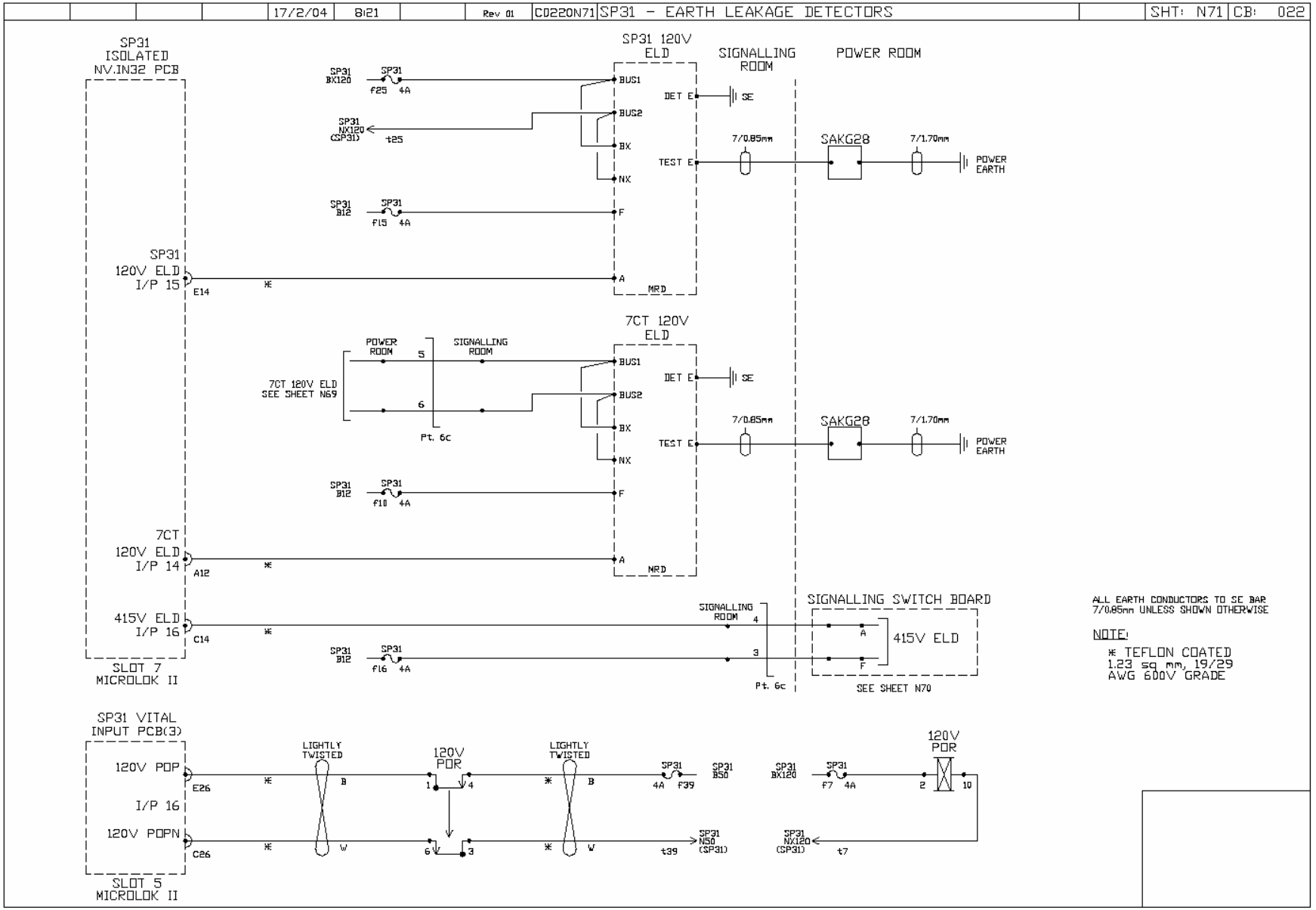
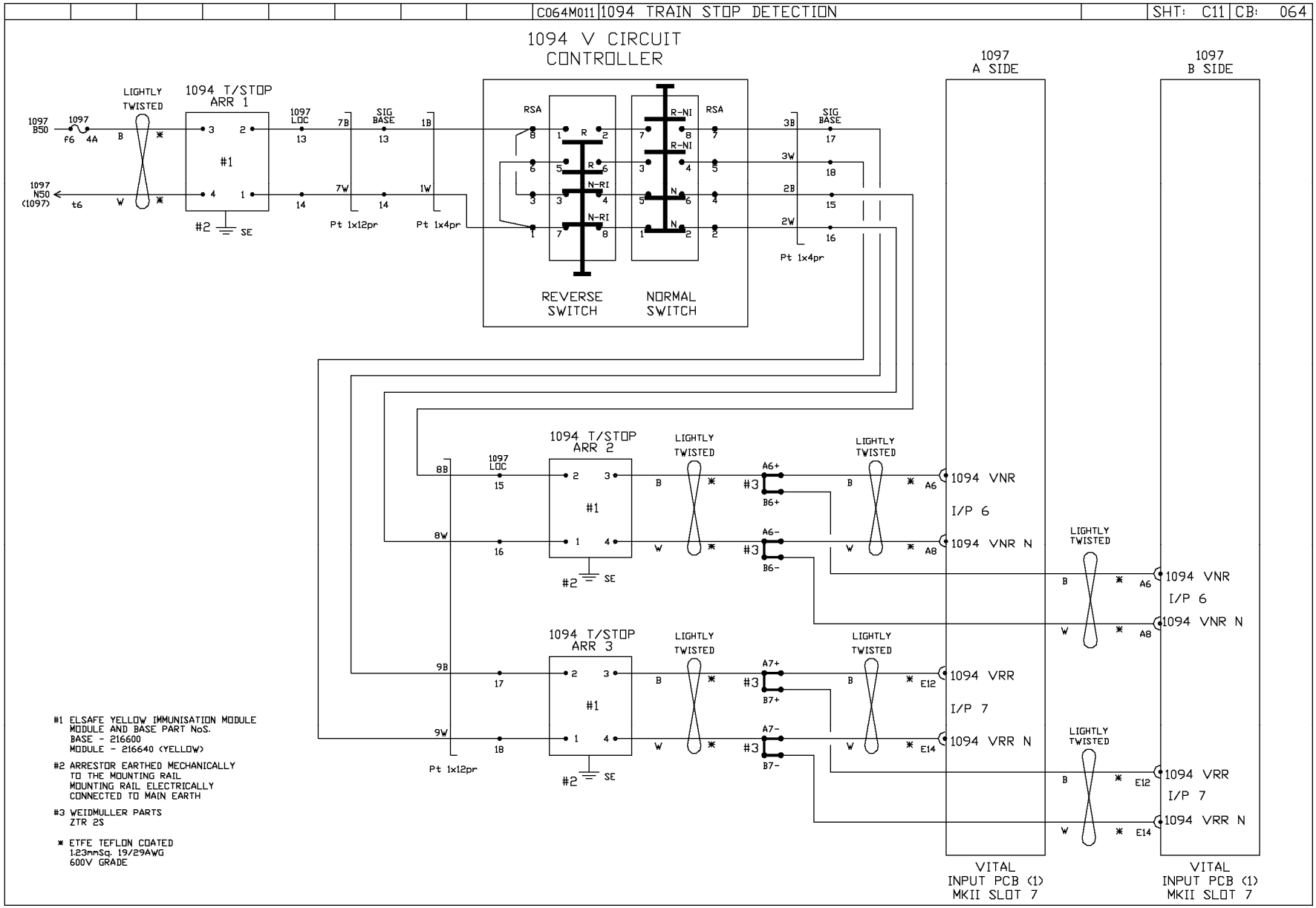
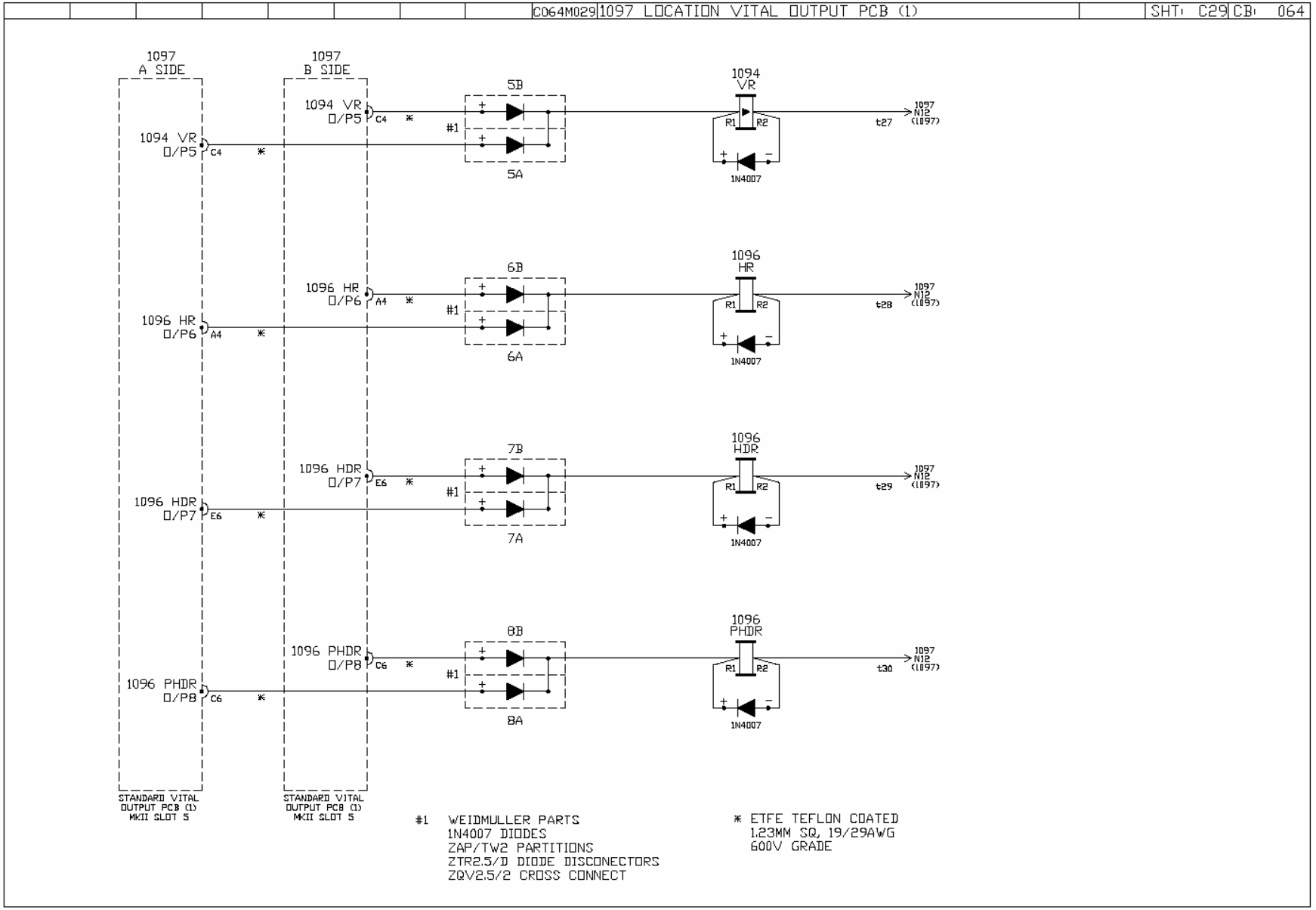
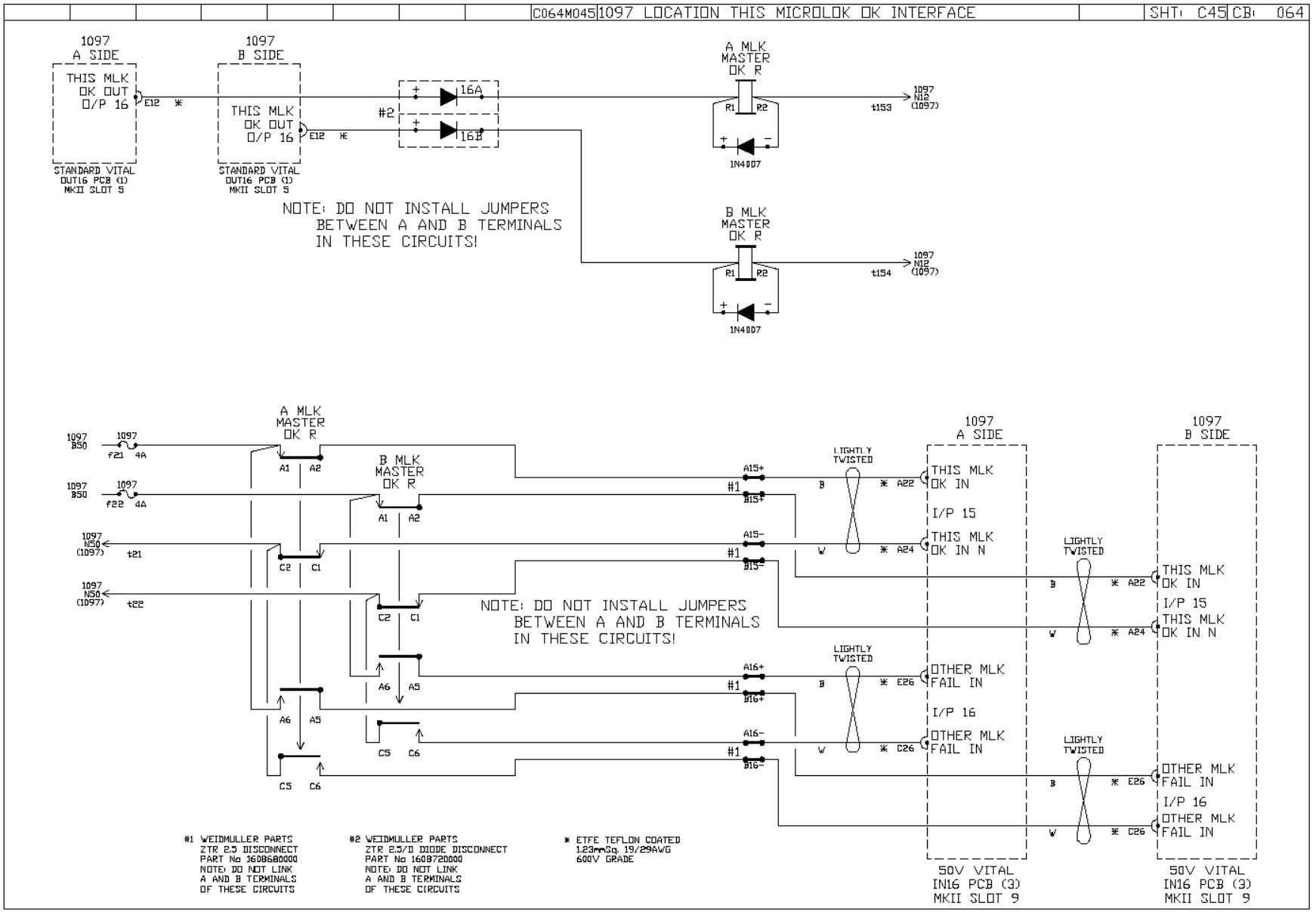
Rev 01
C0220N53
POINTS CONTROL CIRCUITS
SHT: N53
CB: 022
210 EOL
211 EOL
210 EOL IMM 1
210 EOL IMM 2
211 EOL IMM 1
211 EOL IMM 2
SP31 VITAL INPUT PCB(3)
LIGHTLY TWISTED
SP31 B50
SP31 N50 (SP31)
f3 4A
f4 4A
f5 4A
f6 4A
t3
t4
t5
t6
#1
#2
SE
1W Pt 4pr
2W Pt 4pr
210 IR
211 IR
210 EOL I/P 5
210 EOL N
211 EOL I/P 6
211 EOL N
210 ICR I/P 7
210 ICR N
211 ICR I/P 8
211 ICR N
SLOT 5 MICROLOK II
NOTE:
* TEFLON COATED 1.23 sq mm, 19/29 AWG 600V GRADE
#1 ELSAFE IMMUNISATION MODULE AND BASE PART NOS BASE - 216600 MODULE - 216640(YELLOW)
#2 ELSAFE MODULE EARTHED MECHANICALLY VIA THE ATTACHMENT SCREW TO THE MOUNTING RAIL, MOUNTING RAIL ELECTRICALLY CONNECTED TO MAIN EARTH.

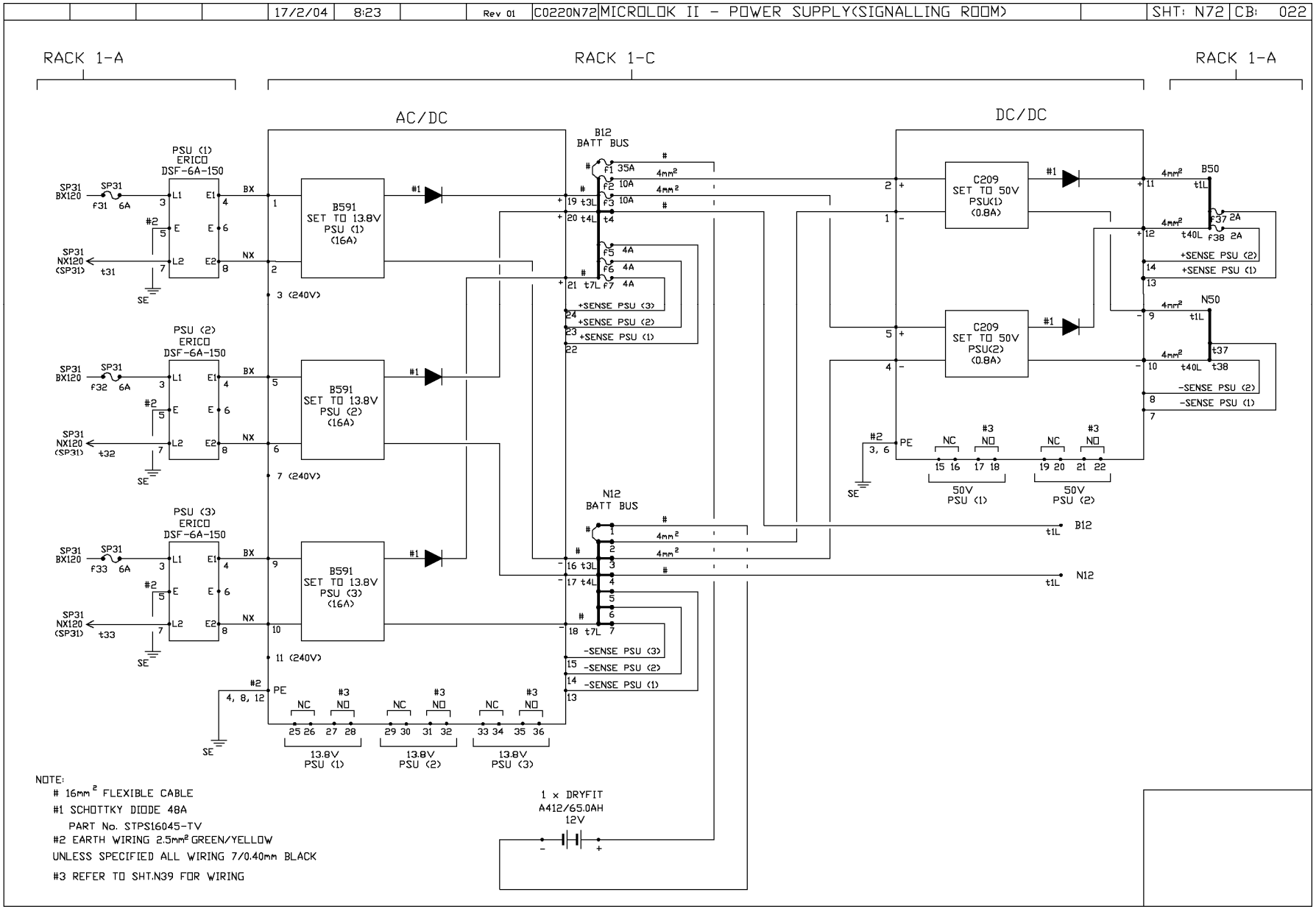

30/9/03
9:58
Rev 01
C0220N68
TRACK REPEAT RELAY CIRCUITS
SHT: N68
CB: 022
33AT R
33(M) HR
33 HDR
33 DR
33AT PR
1N4007
33BT R
31(M) HR
31 HDR
31 DR
33BT PR
1N4007
38AT R
38(M)A HR
38(M)B HR
38(M)A HDR
38(M)B_G JPHDR
38(M)B_B JPHDR
38 DR
38AT PR
1N4007


17/2/04
8121
Rev 01
CD220N71
SP31 - EARTH LEAKAGE DETECTORS
SHT: N71
CB: 022
SP31 ISOLATED NV.IN32 PCB
SP31 120V ELD
SIGNALLING ROOM
POWER ROOM
SP31 BX120
f25 4A
BUS1
BUS2
BX
NX
F
A
MRD
DET E
SE
TEST E
7/0.85mm
SAKG28
7/1.70mm
POWER EARTH
SP31 NX120 (SP31)
t25
SP31 B12
f15 4A
SP31 120V ELD I/P 15
E14
7CT 120V ELD
POWER ROOM
SIGNALLING ROOM
5
6
7CT 120V ELD SEE SHEET N69
Pt. 6c
f10 4A
7CT 120V ELD I/P 14
A12
415V ELD I/P 16
C14
f16 4A
SIGNALLING SWITCH BOARD
415V ELD
SEE SHEET N70
SLOT 7 MICROLOK II
ALL EARTH CONDUCTORS TO SE BAR 7/0.85mm UNLESS SHOWN OTHERWISE
NOTE:
* TEFLON COATED 1.23 sq mm, 19/29 AWG 600V GRADE
SP31 VITAL INPUT PCB(3)
120V POP
I/P 16
120V POPN
E26
C26
LIGHTLY TWISTED
120V POR
SP31 B50
4A F39
t39
SP31 N50 (SP31)
SP31 BX120
F7 4A
t7
SLOT 5 MICROLOK II


C064M011 1094 TRAIN STOP DETECTION
SHT: C11 CB: 064
1094 V CIRCUIT CONTROLLER
1097 A SIDE
1097 B SIDE
LIGHTLY TWISTED
1094 T/STOP ARR 1
1097 B50
1097 N50 (1097)
1097 LOC
SIG BASE
RSA
R-NI
R
N-RI
N
REVERSE SWITCH
NORMAL SWITCH
#1
#2 SE
Pt 1x12pr
Pt 1x4pr
1094 T/STOP ARR 2
1094 T/STOP ARR 3
#3
A6+
B6+
A6-
B6-
A7+
B7+
A7-
B7-
1094 VNR
I/P 6
1094 VNR N
1094 VRR
I/P 7
1094 VRR N
VITAL INPUT PCB (1) MKII SLOT 7
#1 ELSAFE YELLOW IMMUNISATION MODULE
MODULE AND BASE PART NoS.
BASE - 216600
MODULE - 216640 (YELLOW)
#2 ARRESTOR EARTHED MECHANICALLY TO THE MOUNTING RAIL
MOUNTING RAIL ELECTRICALLY CONNECTED TO MAIN EARTH
#3 WEIDMULLER PARTS ZTR 2S
* ETFE TEFLON COATED 1.23mmSq. 19/29AWG 600V GRADE

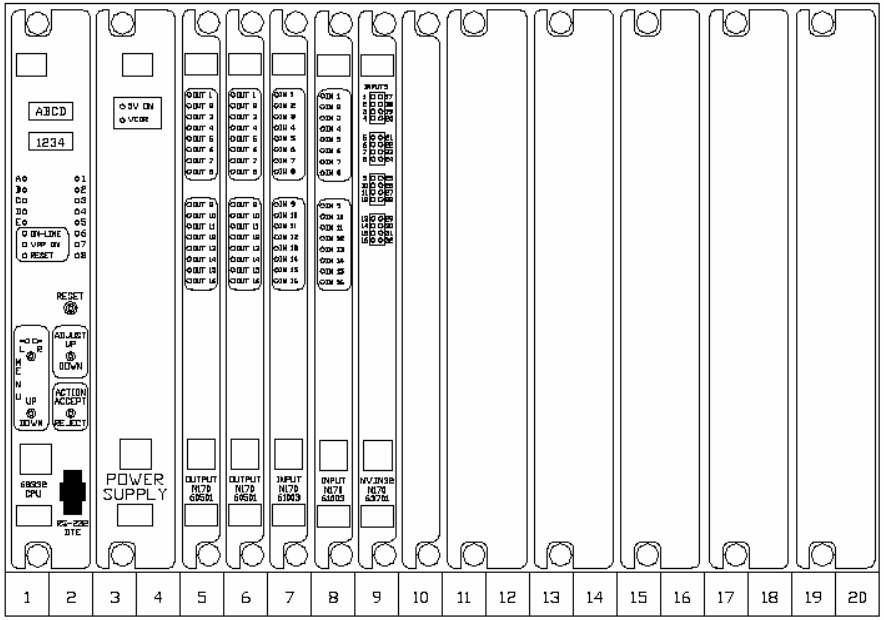

C064M029 1097 LOCATION VITAL OUTPUT PCB (1)
SHT: C29 CB: 064
1097 A SIDE
1097 B SIDE
1094 VR
1096 HR
1096 HDR
1096 PHDR
5B
5A
6B
6A
7B
7A
8B
8A
1N4007
STANDARD VITAL OUTPUT PCB (1) MKII SLOT 5
#1 WEIDMULLER PARTS
1N4007 DIODES
ZAP/TW2 PARTITIONS
ZTR2.5/D DIODE DISCONNECTORS
ZQV2.5/2 CROSS CONNECT
* ETFE TEFLON COATED
1.23MM SQ, 19/29AWG
600V GRADE


C064M045 1097 LOCATION THIS MICROLOK OK INTERFACE
SHT: C45 CB: 064
1097 A SIDE
THIS MLK OK OUT O/P 16
STANDARD VITAL OUT16 PCB (1) MKII SLOT 5
1097 B SIDE
THIS MLK OK OUT O/P 16
STANDARD VITAL OUT16 PCB (1) MKII SLOT 5
#2
16A
16B
A MLK MASTER OK R
B MLK MASTER OK R
1N4007
1097 N12 (1097) t153
1097 N12 (1097) t154
NOTE: DO NOT INSTALL JUMPERS BETWEEN A AND B TERMINALS IN THESE CIRCUITS!
1097 B50 f21 4A
1097 B50 f22 4A
1097 N50 (1097) t21
1097 N50 (1097) t22
A1 A2 C2 C1 A6 A5 C5 C6
#1
A15+ B15+ A15- B15- A16+ B16+ A16- B16-
LIGHTLY TWISTED
THIS MLK OK IN
I/P 15
THIS MLK OK IN N
OTHER MLK FAIL IN
I/P 16
OTHER MLK FAIL IN
* A22 * A24 * E26 * C26
1097 A SIDE
1097 B SIDE
50V VITAL IN16 PCB (3) MKII SLOT 9
#1 WEIDMULLER PARTS ZTR 2.5 DISCONNECT PART No 1608680000 NOTE: DO NOT LINK A AND B TERMINALS OF THESE CIRCUITS
#2 WEIDMULLER PARTS ZTR 2.5/D DIODE DISCONNECT PART No 1608720000 NOTE: DO NOT LINK A AND B TERMINALS OF THESE CIRCUITS
* ETFE TEFLON COATED 1.23mmSq. 19/29AWG 600V GRADE


17/2/04 8:23 Rev 01 C0220N72 MICROLOK II – POWER SUPPLY(SIGNALLING ROOM) SHT: N72 CB: 022
RACK 1-A
RACK 1-C
RACK 1-A
AC/DC
DC/DC
PSU (1) ERICO DSF-6A-150
PSU (2) ERICO DSF-6A-150
PSU (3) ERICO DSF-6A-150
B591 SET TO 13.8V PSU (1) (16A)
B591 SET TO 13.8V PSU (2) (16A)
B591 SET TO 13.8V PSU (3) (16A)
B12 BATT BUS
N12 BATT BUS
C209 SET TO 50V PSU(1) (0.8A)
C209 SET TO 50V PSU(2) (0.8A)
B50
N50
B12
N12
50V PSU (1)
50V PSU (2)
13.8V PSU (1)
13.8V PSU (2)
13.8V PSU (3)
1 x DRYFIT A412/65.0AH 12V
NOTE:
16mm² FLEXIBLE CABLE
#1 SCHOTTKY DIODE 48A
PART No. STPS16045-TV
#2 EARTH WIRING 2.5mm² GREEN/YELLOW
UNLESS SPECIFIED ALL WIRING 7/0.40mm BLACK
#3 REFER TO SHT.N39 FOR WIRING

C064M003 | 1085 LOCATION – MICROLOK CARDFILE LAYOUT A SIDE | PART 1/2 | SHT: B03 | CB: 064

CARDFILE LAYOUT – FRONT



SLOT	BOARD	PART NUMBER
1	CPU	N17061301
2		
3	POWER SUPPLY	N16660301
4		
5	VITAL OUTPUT (12V) 1	N17060501
6	VITAL OUTPUT (12V) 2	N17060501
7	VITAL INPUT (50V) 1	N17061003
8	VITAL INPUT (50V) 2	N17061003
9	NON-VITAL ISOLATED INPUT	N17063701
10	1 WIDE BLANKING PLATE	N451850-2902
11	2 WIDE BLANKING PLATE	N451859-2901
12		
13	2 WIDE BLANKING PLATE	N451859-2901
14		
15	2 WIDE BLANKING PLATE	N451859-2901
16		
17	2 WIDE BLANKING PLATE	N451859-2901
18		
19	2 WIDE BLANKING PLATE	N451859-2901
20		

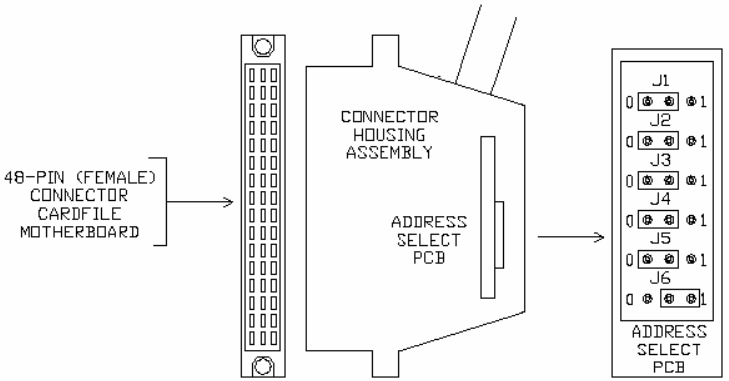
KEYING PLUG LOCATION: 1 2 3 4 5 6 7 8 9 10 11 12

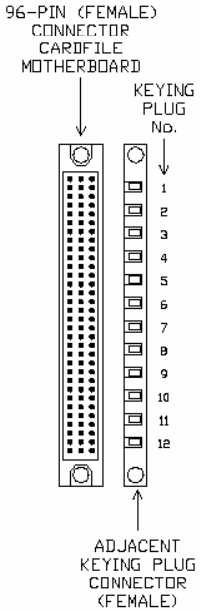
ADDRESS JUMPER SETTING (0=OPEN, 1=CLOSED): 1 2 3 4 5 6

5	○	○	○	○	○	1
6	○	1	○	○	○	1
7	○	○	1	○	○	1
8	○	1	1	○	○	1
9	○	○	○	1	○	1

MICROLOK II
(PART NO: N16902101)

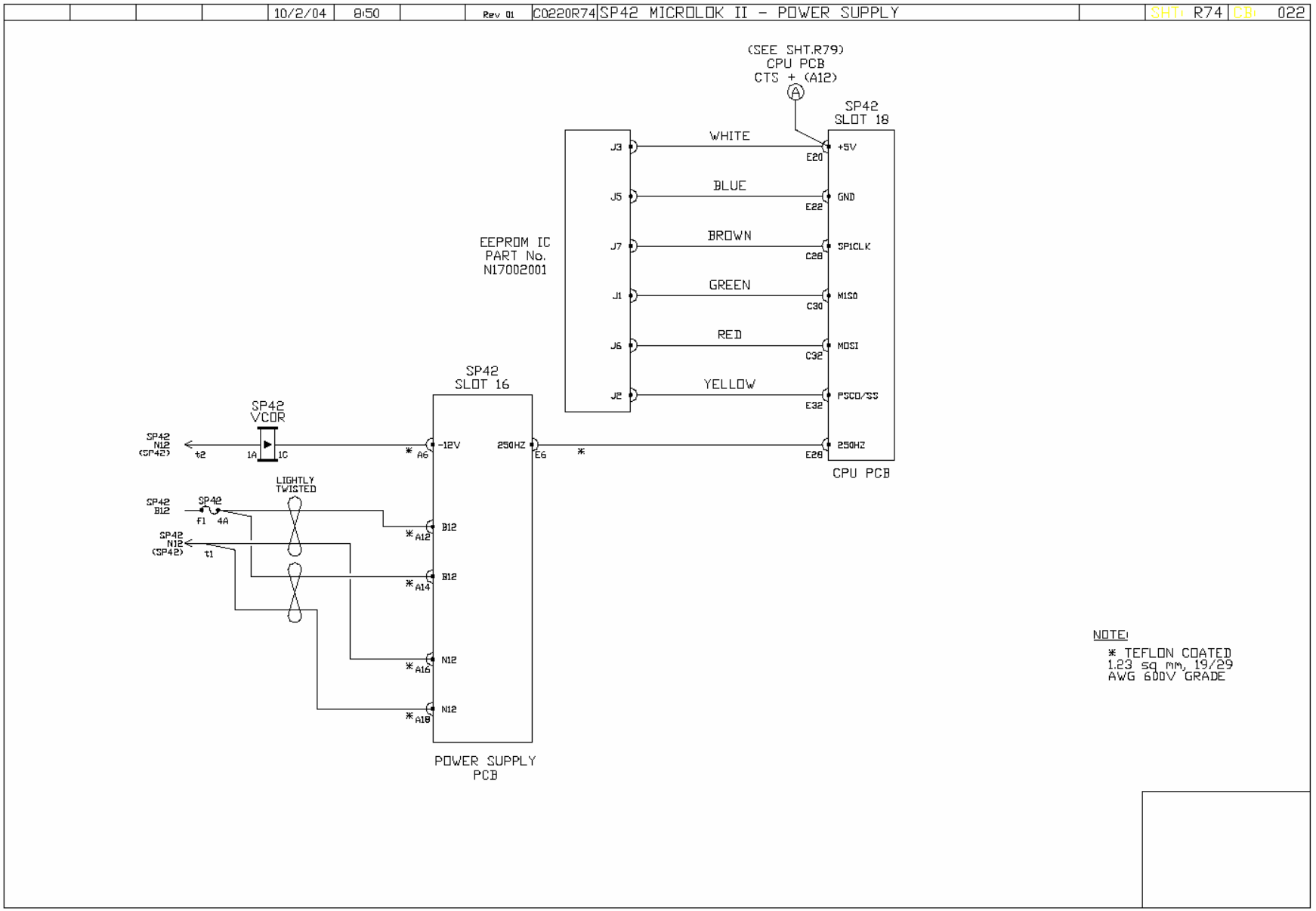
NOTE: SPARE SLOTS MUST BE COVERED WITH BLANKING PLATES

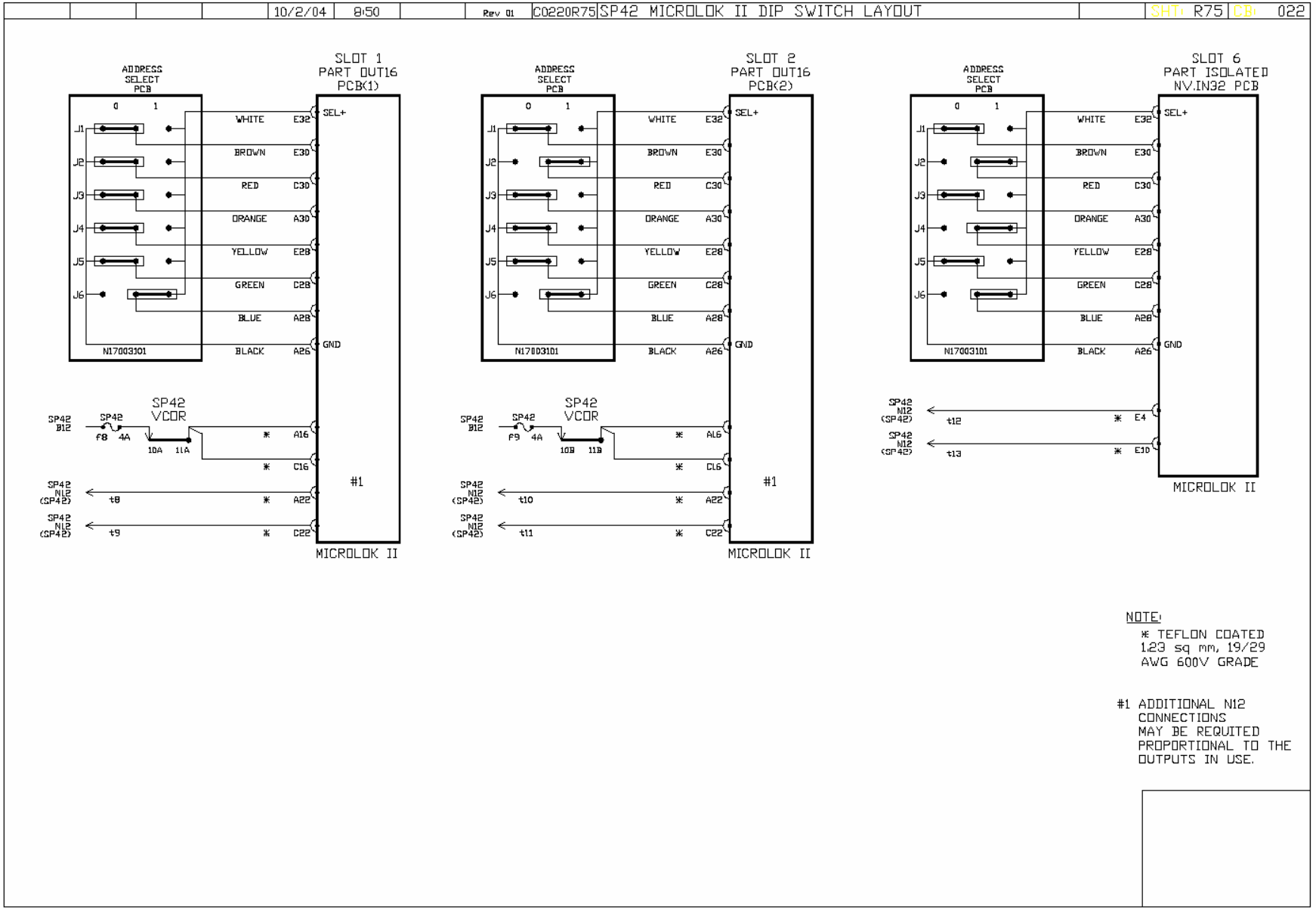


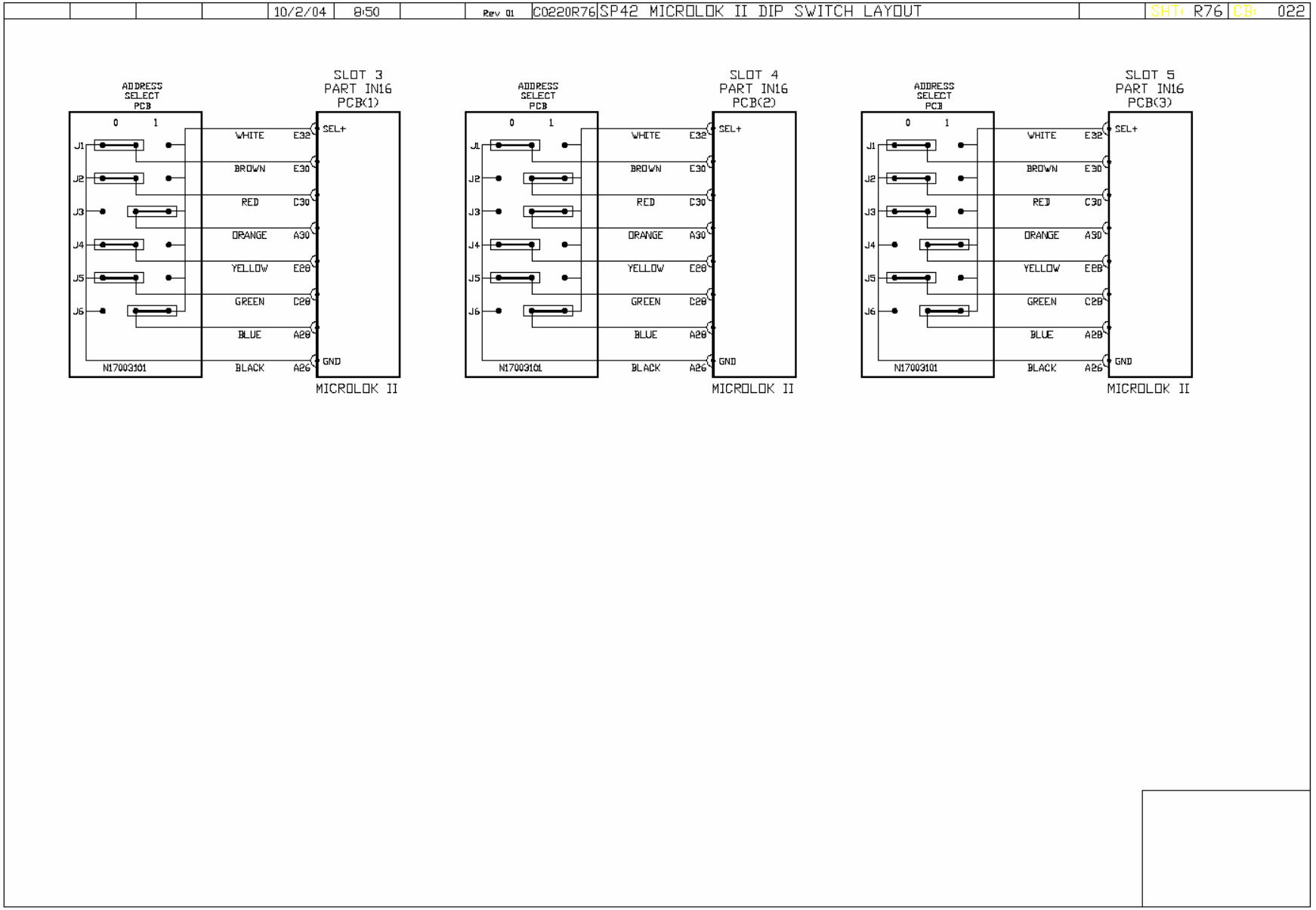


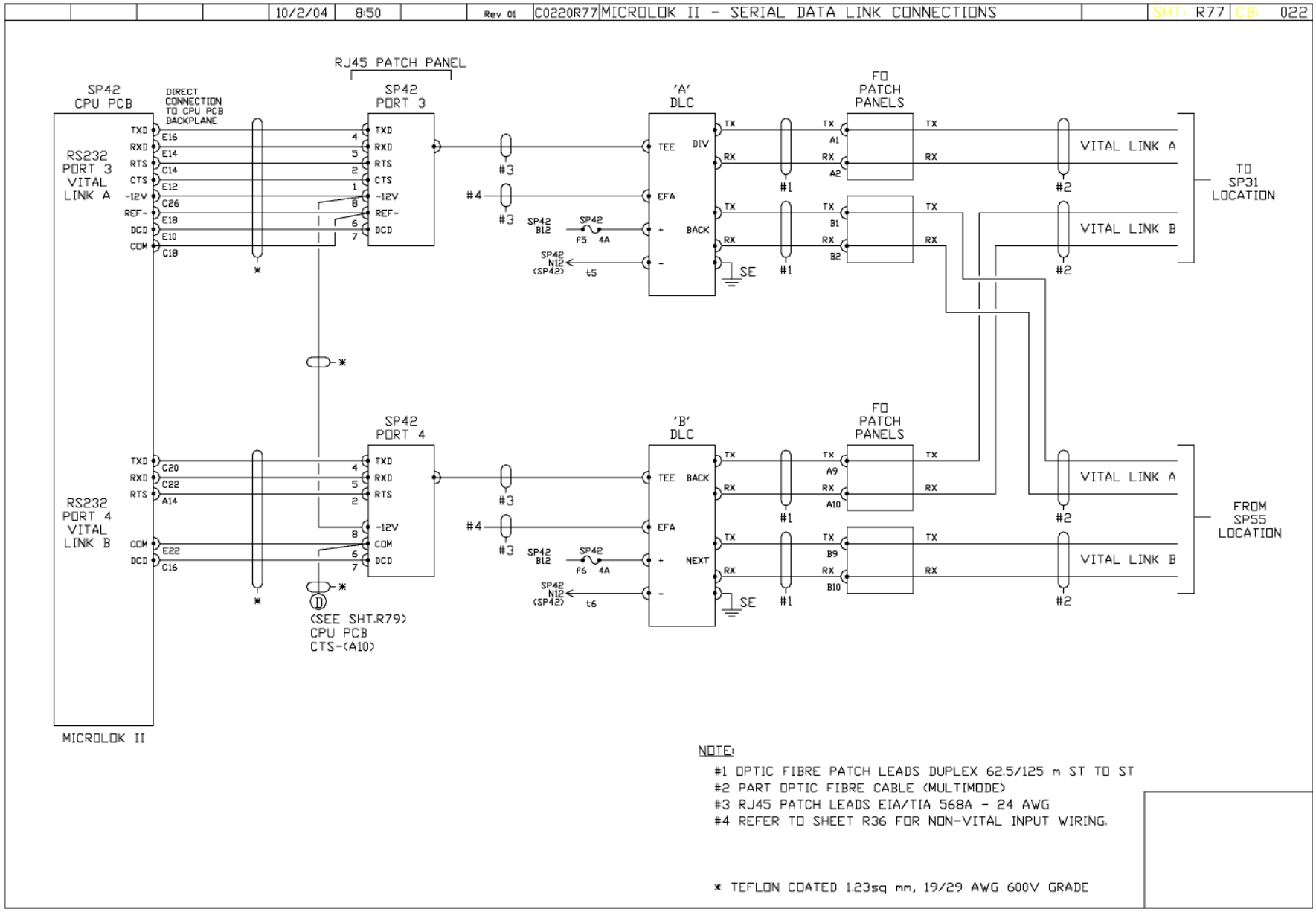
CPU INDICATION	
LED No.	FUNCTION
1	COMMUNICATION ON LINK 1 NORMAL
2	SPARE
3	COMMUNICATION ON LINK 3 NORMAL
4	COMMUNICATION ON LINK 4 NORMAL
5	COMMUNICATION ON LINK 5 NORMAL
6	SPARE
7	SPARE
8	SPARE

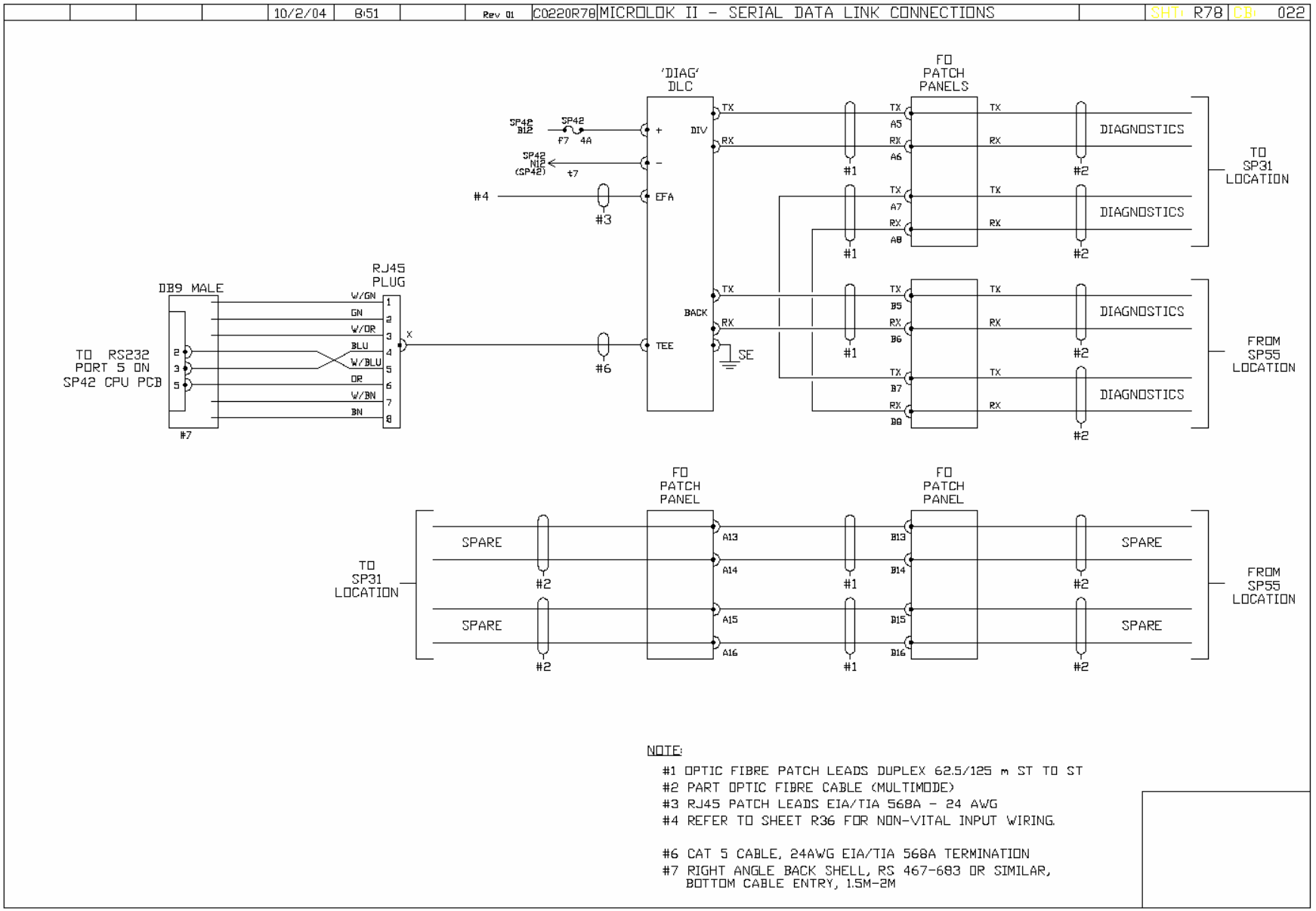
● INDICATES KEYING PLUG INSERTED

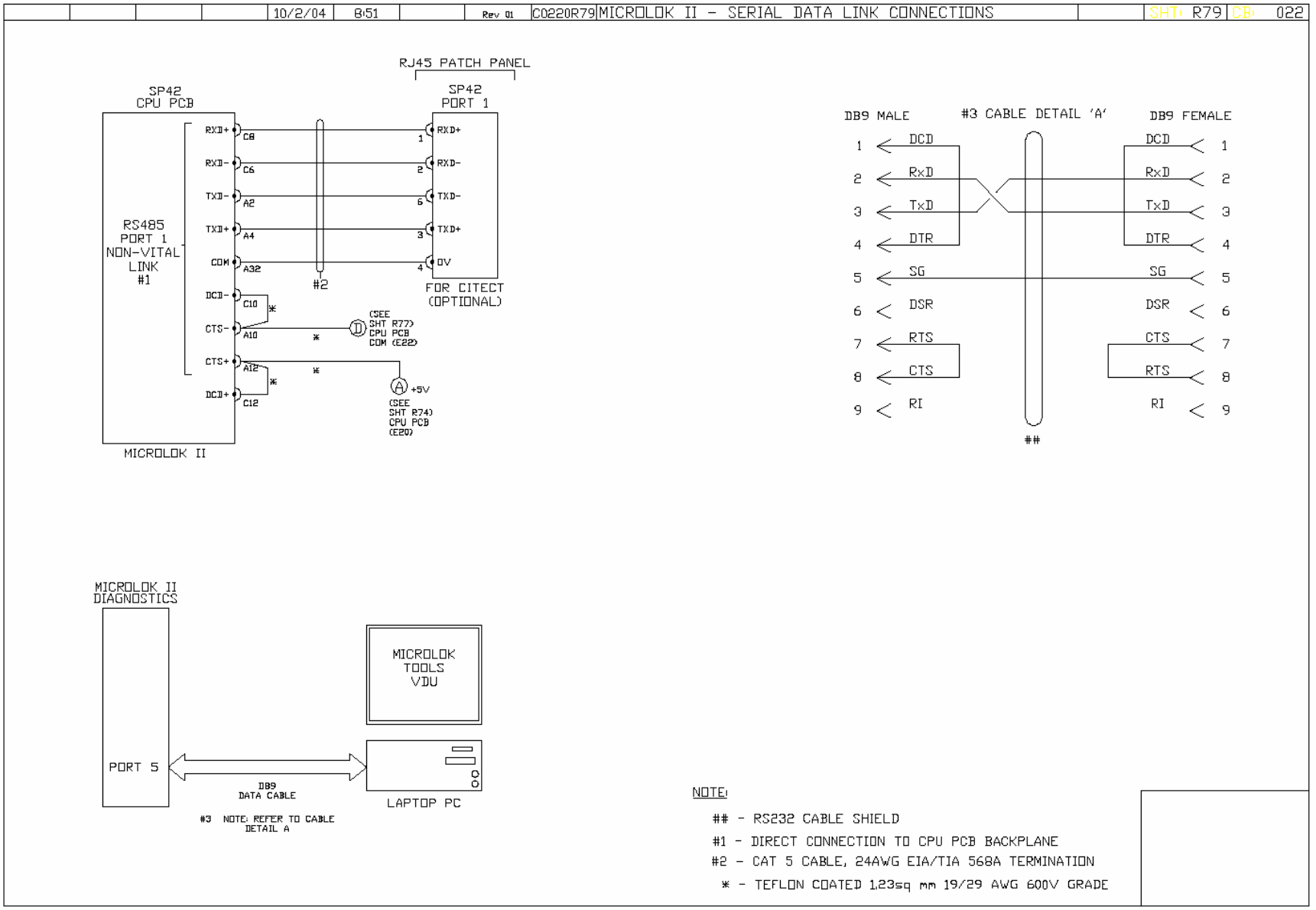

10/2/04
8:50
Rev 01
C0220R74
SP42 MICROLOK II - POWER SUPPLY
SHT: R74
CB: 022
(SEE SHT.R79)
CPU PCB
CTS + (A12)
A
SP42
SLOT 18
WHITE
BLUE
BROWN
GREEN
RED
YELLOW
J3
J5
J7
J1
J6
J2
E20
E22
E28
E30
E32
+5V
GND
SPICLK
MISO
MOSI
PSCO/SS
250HZ
EEPROM IC
PART No.
N17002001
SP42
SLOT 16
SP42
VCOR
SP42
N12
(SP42)
t2
1A
1C
-12V
A6
E6
E26
CPU PCB
LIGHTLY
TWISTED
SP42
B12
SP42
F1
4A
SP42
N12
(SP42)
t1
B12
A12
B12
A14
N12
A16
N12
A18
POWER SUPPLY
PCB
NOTE:
* TEFLON COATED
1.23 sq mm, 19/29
AWG 600V GRADE


10/2/04
8:50
Rev 01
C0220R75
SP42 MICROLOK II DIP SWITCH LAYOUT
SHT: R75
CB: 022
ADDRESS SELECT PCB
SLOT 1 PART OUT16 PCB(1)
SLOT 2 PART OUT16 PCB(2)
SLOT 6 PART ISOLATED NV.IN32 PCB
N17003101
WHITE
BROWN
RED
ORANGE
YELLOW
GREEN
BLUE
BLACK
SEL+
GND
SP42 VCOR
MICROLOK II
#1
NOTE:
* TEFLON COATED 1.23 sq mm, 19/29 AWG 600V GRADE
#1 ADDITIONAL N12 CONNECTIONS MAY BE REQUITED PROPORTIONAL TO THE OUTPUTS IN USE.


10/2/04
8:50
Rev 01
C0220R76
SP42 MICROLOK II DIP SWITCH LAYOUT
SHT: R76
CB: 022
SLOT 3
PART IN16
PCB(1)
SLOT 4
PART IN16
PCB(2)
SLOT 5
PART IN16
PCB(3)
ADDRESS
SELECT
PCB
0
1
J1
J2
J3
J4
J5
J6
WHITE
BROWN
RED
ORANGE
YELLOW
GREEN
BLUE
BLACK
E32
E30
C30
A30
E28
C28
A28
A26
SEL+
GND
N17003101
MICROLOK II


10/2/04 8:50 Rev 01 C0220R77 MICROLOK II - SERIAL DATA LINK CONNECTIONS SHT: R77 CB: 022
RJ45 PATCH PANEL
SP42 CPU PCB
DIRECT CONNECTION TO CPU PCB BACKPLANE
RS232 PORT 3 VITAL LINK A
TXD E16
RXD E14
RTS C14
CTS E12
-12V C26
REF- E18
DCD E10
COM C18
SP42 PORT 3
'A' DLC
TEE DIV
EFA
+ BACK
-
SE
FO PATCH PANELS
VITAL LINK A
VITAL LINK B
TO SP31 LOCATION
#1
#2
#3
#4
SP42 B12
SP42 N12 (SP42)
f5 4A
t5
RS232 PORT 4 VITAL LINK B
TXD C20
RXD C22
RTS A14
COM E22
DCD C16
SP42 PORT 4
'B' DLC
TEE BACK
EFA
+ NEXT
-
SE
f6 4A
t6
FROM SP55 LOCATION
(SEE SHT.R79) CPU PCB CTS-(A10)
MICROLOK II
NOTE:
#1 OPTIC FIBRE PATCH LEADS DUPLEX 62.5/125 m ST TO ST
#2 PART OPTIC FIBRE CABLE (MULTIMODE)
#3 RJ45 PATCH LEADS EIA/TIA 568A - 24 AWG
#4 REFER TO SHEET R36 FOR NON-VITAL INPUT WIRING.
* TEFLON COATED 1.23sq mm, 19/29 AWG 600V GRADE


10/2/04
8:51
Rev 01
C0220R78
MICROLOK II – SERIAL DATA LINK CONNECTIONS
SHT: R78
CB: 022
'DIAG' DLC
FO PATCH PANELS
DIAGNOSTICS
TO SP31 LOCATION
FROM SP55 LOCATION
RJ45 PLUG
DB9 MALE
TO RS232 PORT 5 ON SP42 CPU PCB
W/GN
GN
W/OR
BLU
W/BLU
OR
W/BN
BN
#1
#2
#3
#4
#6
#7
EFA
TEE
BACK
DIV
SE
TX
RX
SPARE
NOTE:
#1 OPTIC FIBRE PATCH LEADS DUPLEX 62.5/125 m ST TO ST
#2 PART OPTIC FIBRE CABLE (MULTIMODE)
#3 RJ45 PATCH LEADS EIA/TIA 568A – 24 AWG
#4 REFER TO SHEET R36 FOR NON-VITAL INPUT WIRING.
#6 CAT 5 CABLE, 24AWG EIA/TIA 568A TERMINATION
#7 RIGHT ANGLE BACK SHELL, RS 467-683 OR SIMILAR, BOTTOM CABLE ENTRY, 1.5M-2M


10/2/04
8:51
Rev 01
C0220R79
MICROLOK II - SERIAL DATA LINK CONNECTIONS
SHT: R79
CB: 022
RJ45 PATCH PANEL
SP42
CPU PCB
SP42
PORT 1
RS485
PORT 1
NON-VITAL
LINK
#1
RXD+
RXD-
TXD-
TXD+
COM
DCD-
CTS-
CTS+
DCD+
C8
C6
A2
A4
A32
C10
A10
A12
C12
1
2
6
3
4
RXD+
RXD-
TXD-
TXD+
0V
#2
FOR CITECT
(OPTIONAL)
(SEE
SHT R77)
CPU PCB
COM (E22)
+5V
(SEE
SHT R74)
CPU PCB
(E20)
MICROLOK II
DB9 MALE
#3 CABLE DETAIL 'A'
DB9 FEMALE
1 DCD
2 RxD
3 TxD
4 DTR
5 SG
6 DSR
7 RTS
8 CTS
9 RI
##
MICROLOK II
DIAGNOSTICS
PORT 5
DB9
DATA CABLE
MICROLOK
TOOLS
VDU
LAPTOP PC
#3 NOTE: REFER TO CABLE
DETAIL A
NOTE:
- RS232 CABLE SHIELD
#1 - DIRECT CONNECTION TO CPU PCB BACKPLANE
#2 - CAT 5 CABLE, 24AWG EIA/TIA 568A TERMINATION
* - TEFLON COATED 1.23sq mm 19/29 AWG 600V GRADE

8. Appendix B – Hot Standby Arrangements

SIGNAL DESIGN

MICROLOK II
DUAL HOT STANDBY ARRANGEMENTS

1. Introduction

The hot standby configurations are used to maximise the availability of signal interlockings as required by the application or site.

Configurations are based on interlocking masters and slaves. The interlocking slaves manage the physical vital inputs and outputs. The interlocking masters perform the signalling safety logic processing.

Hot standby configurations are based on duplicated interlocking masters, with either non-duplicated slaves or fully duplicated slaves.

Redundant communications links are provided for each type of hot standby configuration.

In the case of duplicated masters and non-duplicated slaves, the masters shall not have any vital input or output cards installed.

The diagnostics port (5) of all slave locations are connected back to a diagnostics PC near the masters.

1.1 Conventions

In this portion of the document, which specifically covers the ARTC implementation of Dual Hot Standby systems of Microlok II interlockings, please be aware of the following notes and conditions.

1.1.1 Generality of Serial Communication Ports

With the exception of the diagnostics serial port (port 5), where reference is made to specific ports in the following material, the ports referenced will be those applicable to a typical implementation of the Dual Hot Standby system. As will be described later, port 3 is typically used for communicating with slave locations, and port 4 is typically connected to the control system. This is because these ports are most easily interfaced to modems for communicating with equipment in other locations, and port 3 has higher priority than port 4. This leaves ports 1 and 2 for the “dual link”.

However, some interlockings may be subject to specific circumstances or constraints in which different allocation of ports may be beneficial. One likely example is where masters communicate with multiple slaves which are all in the same room as the master. Here, port 1 or 2 may be used for the slave communications. These ports are capable of providing a multi-drop communications link without additional equipment, which reduces cost, space requirements, and may improve the response times on the communications link. Having higher priority, port 1 is preferred for the vital link to the slaves. Port 2 would be used for the control systems link, but either a modem with RS-485 interface , or a RS-232 – RS-485 converter, is required. Ports 3 and 4 are then used for the dual link.

Such re-allocation of the serial ports is permissible, but the designer must be aware that not all ports are compatible with each other (without converters) for use on the dual link. Hence the dual link uses ports 1 and 2 or ports 3 and 4.

2. Control System interface

The Control System will communicate to the Interlocking Masters using a Genisys protocol.

The Control System may be duplicated, including a dual or "Master" and "Standby" system. Both sides of the dual control system shall send controls and receive indications from the Interlocking masters.

Only the side of Control System that is "Master" processes the bits received from the Interlocking Master.

The Control System will determine mastership by two means, firstly by manual control and secondly by arbitration based on a health calculation.

The Control System must ensure it is receiving the "On Standby" status from the Interlocking Master prior to switching that Interlocking Master to "On Line" status.

Mastership, or "On Line" status will be provided by sending the "Control System Master" bit to the Interlocking Master that is to go on line.

Failures of power supplies or the dual link (ports 1 or 2) connection between the two Interlocking Masters will raise an alarm but not cause the switching of mastership between the two Interlocking Masters.

A complete failure of the Interlocking Master that is on line, a failure of that interlockings port 4 connection to the Control System, or a loss of “On Standby”status must result in the switching of mastership between the Interlocking Masters.

The Control System must detect failure of communications to an interlocking master and respond in less than one-half the stale data timeout set for the dual link between the interlocking masters. The stale data timeout is normally set to 4 seconds.

In a multiple failure situation where failures exist in the data link communications to the slave locations the switching of mastership between the Interlocking Masters will be dependant on the arbitration based on health calculations.

The Control System will be provided with the necessary health status of all the required equipment including Interlocking Master and Slave cardfiles and all intermediate communications equipment to allow the health calculations to be performed. Generally, alarms and indications should be available to ATRICS from both interlocking masters. In particular, the status of the link between the master and the slaves needs to be passed across the dual link of the interlocking, and both masters will send THIS_PORT_3_OK and OTHER_PORT_3_OK to ATRICS.

The Control System will also be provided with indications of the following functions; MASTER ON LINE, ON STANDBY, DUAL LINK OK, CPS.STATUS, and MICROLOK WARNING where provided. Each master should only send its own indications of these functions, there is no need to send indications of the other master’s status.

3. Interlocking Masters

3.1 General

Identical application data shall be installed in Interlocking Master A and Interlocking Master B. Different configurable settings are acceptable only when they directly relate to Hot Standby functionality.

Hot standby application data uses the concept of the “A” prefix to mean “this” interlocking , the “B” prefix to mean “the other” interlocking.

The two Interlocking Masters utilise two serial ports, typically ports 1 and 2, to establish two connetions between each other. Port 2 (master) of one interlocking is connected to port 1 (slave) of the other interlocking and vice versa. Port 1 sends outputs only and port 2 receives inputs only. This will be known as the dual link and is provided to allow the synchronisation of the two Interlocking Masters to be achieved.

The Interlocking Masters typically utilise port 3 to communicate with the interlocking slaves.

Each Interlocking Master receives the same inputs/indications from the field (Slave Locations) via port 3. These inputs are also sent as outputs to "the other" Interlocking Master via port 1.

The inputs received at port 2 are OR’d with those inputs received at port 3. Having the slave location inputs available at both ports will enable the Interlocking Master on line to continue to function independent of any communication link failure between the two Interlocking Masters or between the Interlocking Masters and the slave locations.

Should a failure of the dual link occur the Interlocking Master that is not “online master” shall not be able to send outputs. With the dual link failed, a separate interface between the two sides must be used to determine whether the link failure is a failure of the link only, or if the other master has failed. Different methods are used depending on the slave arrangements, and are discussed later.

Each Interlocking Master has a separate connection to the Control System via a serial link, typically port 4. The Interlocking Masters are Genisys slaves of the Control System master.

Because identical data is installed in each Interlocking Master, both masters will be capable of communicating identically with the Control System. The control system will determine which Interlocking Master is to be placed “online”, and will send the “Control System Master” bit to that master only. During mastership changeover, the control system will be sending “Control System Master” to both Interlocking Masters for a short period. All other control bits may be sent either to the online master only, or identically to both masters. Control bits will only be accepted when the control system link is proven OK.

Except for a short period after a reset, each Interlocking Master will continually send indication bits to the control system.

The Interlocking Masters will receive the interlocking address via the first 8 input data bits of the communication link of each Slave location. The interlocking address is then confirmed prior to each of the remaining input data bits being processed.

The CPU Executive version number must be entered under system configuration of the Microlok II tools program to ensure both Interlocking Masters are running on the same version of software. Also the entered data version is converted to a binary number within the application data and sent via the dual link for comparison to ensure both Interlocking Masters are functioning on the same version of data.

The particular safety issues are:

Crossed vital Serial links, which is managed by having identical data for each interlocking address, and slave address combination.

Different data in each master is managed by checking an address for the application data against the card file, and cross checking the application data version number against that supplied by the other interlocking master.

Slow response due to stale data timeout, and intermittent operation of link due to bits being held for the stale data timeout. This is managed by ensuring that the links are in good condition with a low error rate (<1 in 1000 messages) and setting the stale data timeout to 2.5 times the poll rate for slaves on the link.

Possibility of "lost" track occupancies due to slow comms links. The combined effect of slow pick timers on track circuit input bits and the stale data timeout makes this unlikely. Timers are applied to track circuits such that all track circuit types will be 3 seconds slow to pick. For track circuit occupancy to be lost, the tack would have to be occupied then unoccupied , and the 3 second timer expire, in the time between the communications failing and the stale data timeout clearing all bits on that link. Careful analysis of this possibility will be required where fast short trains operate over short track circuits and the stale data timeout is longer than 4 seconds.

Un-synchronised interlocking or interlocking that should not be online issuing controls or turning outputs ON. May be due to routes not set, logic containing stick paths, or points setting. This is managed by application design procedures (rules, review, verification, and testing), comparison when the dual link is functional requiring interlockings to agree before outputs are set, and forced suspension of output processing in the master which is not online if the dual link fails.

Proving the operational (or non-operational) status of the other master during a Dual Link failure is achieved by ONLY_ONE_MASTER logic. The implementation varies based on the configuration of the slaves.

Slave safety issues, which are discussed in the section on slaves.

3.2 Masters Split into Two Cardfiles

In some cases the interlocking master needs to be split to handle the quantity of safety logic. The Masters are broken into MP1 and MP2 card files.

MP1 performs the controls and locking functions. MP2 performs the outputs functions to the slaves.

The hot standby logic must be in the MP1 card file so that the Control System can change the ON LINE status within the stale data timeout of the dual link.

At all external interfaces, MP1 and MP2 must appear as a single unit. If one processor fails, the other processor of that side must present a failed status on remaining communications links. If MP2 fails, the control system must see MP1 not available to be Master. If MP1 fails, MP2 must provide some indication of this to slaves so that the other master can achieve ONLY_ONE_MASTER.

BOOT UP JR is to include the CPS.STATUS for MP1 and MP2 cardfiles. DUAL LINK OK is to include the dual link ports for MP1 and MP2 cardfiles.

4. Slave Locations

4.1 General

The interlocking masters communicate with the interlocking slaves via Microlok vital serial protocol links.

A slave location will receive the interlocking address via the first 8 input data bits. The interlocking address is to be confirmed prior to processing all data bits from the masters See section 6 for Microlok data "Equivalent Circuits" for further information on Interlocking Addressing.

Bits from the masters to drive outputs are OR'd, and inputs from the field equipment are sent to both masters. The slaves perform only limited processing of data. Track circuit inputs are given slow pick repeats before being sent to the masters. Trainstop drive, where required, may be derived from the HR and the first track in the slave, and the train stop proved reverse in the HR output.

The particular safety issues are:

Crossed vital Serial links which is managed by having identical data for each interlocking address, and slave address combination.

Different data from each master which is managed by same application data, synchronisation of the masters, and comparison by ANDing the master outputs before sending.

Different application data in dual slaves. This is managed by procedures.

Slow response due to stale data timeout, and intermittent operation of link due to bits being held for stale data timeout. This is managed by ensuring that the links are in good condition with a low error rate (<1 in 1000 messages) and setting the stale data timeout to 2.5 times the poll rate for slaves on the link.

Twice the wrong side failure rate for inputs. Accepted.

Twice the wrong side failure rate for outputs. Accepted.

4.2 Interface Between Two Interlockings

A slave location may be used as an interface point between two adjacent signalling interlockings. This slave location where required will allow locking from the adjacent signal interlockings to be effective. This Slave location may require two interlocking addresses.

The interface location will typically be more closely associated with one interlocking (primary) than the other (secondary). The connection to the primary interlocking will be by the same port(s) as all other slaves, and the connection to the secondary interlocking will be by alternate ports as available.

5. System Hardware configurations

5.1 Interlockings with No Slaves

This arrangement will generally only be used for very small interlockings.

With the exception of those related to the hot standby arrangement, physical inputs will be wired in parallel, and outputs will be OR'd by a diode circuit.

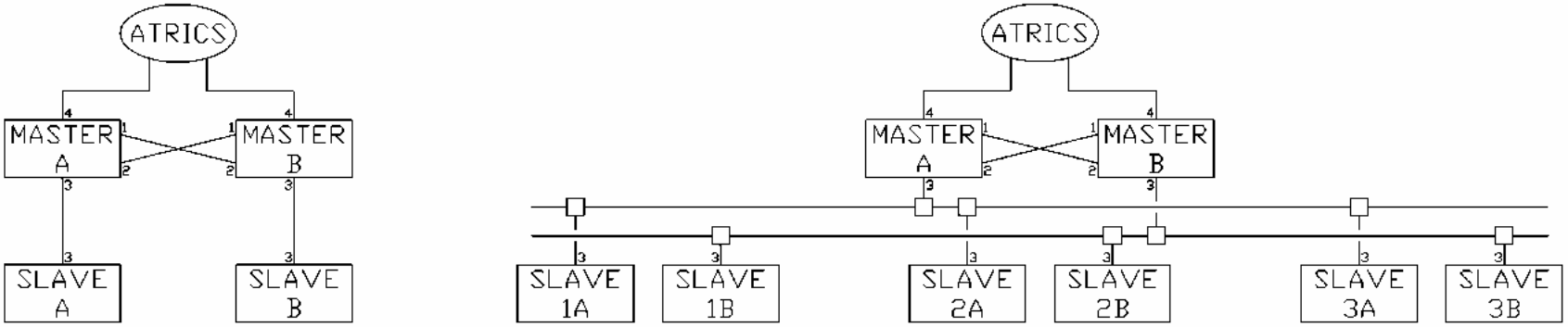
The particular safety issues are:

The cross proving of the other master being failed – the possibility of a master being operational but being perceived by the other master to have failed. See section 5.4 for the THIS_MLK_OK interface to provide failure proving.

Reliability Issues:

Wiring fault in the THIS_MLK_OK interface means failure of other side is not proven. Some modes of this failure will be detected by the loss of THIS_MLK_OK_IN on the affected side. Otherwise, this is a secondary failure.

5.2 Interlockings with Duplicated Slaves



This is essentially an extension of the "no slaves" configuration. As shown in the diagrams, it may consist of a single pair of slaves in the same location as the masters, or several slave pairs in many locations. Where multiple slave locations exist, they will usually be connected by fibre optic communications links utilising either Fibre Optic Modem Sets (FOMS), or where required according to section 2.6 of the specification "Design of Microlok Interlockings", a loop arrangement with Diversity Link Controllers (DLC).

Typically port 3 of the A slave will be connected to the Interlocking Master A, and port 3 of the B slave will be connected to the Interlocking Master B. There is no direct link between the slaves.

There shall be no vital output cards installed in the master cardfiles. Vital input cards may be installed in the masters, but are not preferred.

The application data installed in duplicated slaves shall be the same for both A and B slaves. The configuratrion and bit allocations are to be identical for the slaves.

External inputs are connected in parallel to both slaves, which are then sent to the masters.

Outputs from both slaves are diode OR'd together.

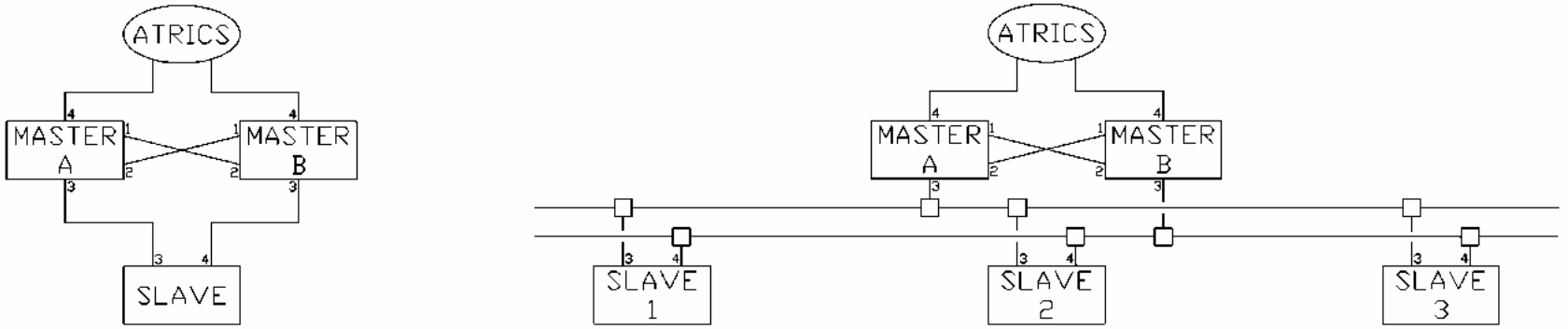
The particular safety issues are:

As for the No Slaves arrangement.

Reliability Issues:

Slaves used for cross proving of interlocking masters become critical for system availability, as failure of the particular slave will result in that interlocking master losing ON_STANDBY status. Generally acceptable. Where analysis has determined this is not acceptable, THIS_MLK_OK interfaces may be provided on multiple slaves and OR'd in the masters.

5.3 Interlockings with Non-duplicated Slaves



As shown in the diagrams, it may consist of a single slave in the same location as the masters, or several slaves in many locations. Where multiple slave locations exist, they are to be connected by fibre optic communications links utilising either Fibre Optic Modem Sets (FOMS), or where required according to section 2.6 of the specification "Design of Microlok Interlockings", a loop arrangement with Diversity Link Controllers (DLC).

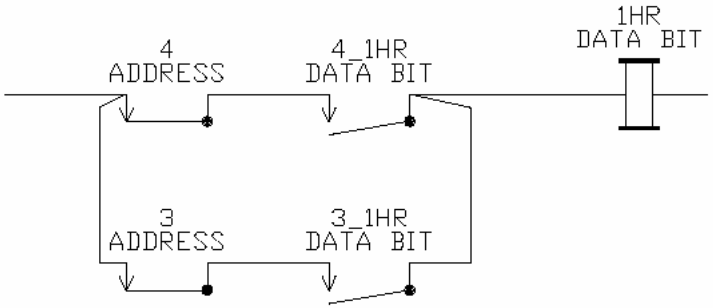
With each slave connected to both masters by vital link, proof that the other Master is not controlling the slaves is provided by vital link status from the slaves.

There shall be no vital input or output cards installed in the master cardfiles.

The slave will typically interface with the master by ports 3 and 4. The configuration and bit allocations shall be identical. The information sent via port 3 will be processed by Interlocking Master A, and the information sent via port 4 will be processed by Interlocking Master B. Inputs received at port 3 are to be prefixed with "3" and inputs received at port 4 are to be prefixed with "4".

Outputs to the interlocking masters are to be sent on both ports.

The received bits are to be OR'd before being processed to allow inputs from either port to work. The example below of 1HR demonstrates the processing of bits from the master for output.



Reliability Issues:

Failure of a slave will immediately result in failure of trackside equipment. Equipment must be grouped to slaves in order to meet the requirements of section 2.2 of the specification "Design of Microlok Interlockings".

5.4 Failure Proving in Fully Duplicated Systems

Where the system with non-duplicated slaves can use the slaves to determine whether or not a dual link failure is due to the failure of the other master, this is not possible in a fully duplicated system. Duplicated systems – either with no slaves or with duplicated slaves – use a hard-wired interface to provide the required proving of the other Microlok.

Each master generates a health bit. This bit drives a vital output, either on the master of a no slaves system, or on one (or more) of the slaves. This bit is not compared with the equivalent bit on the other side before it is sent to the output. The vital output is named THIS_MLK_OK_OUT. It is not diode OR'd with the output from the other side, but each side drives its own Q-type relay: A MLK OK or B MLK OK as appropriate.

Back contacts of this relay are fed to a vital input of the other side – OTHER_MLK_FAIL_IN. If the A side fails, the A MLK OK relay drops out, and the B side receives the input OTHER_MLK_FAIL_IN, providing assurance that the dual link has failed because the A side has failed.

To protect against scenarios where the relay may be down due to other causes, such as the coil buring out or the slave failing, front contacts of the relay are fed back into the Microlok which drives the relay as THIS_MLK_OK_IN. If the Microlok does not receive this indication that the interface circuit is intact, it will generate a warning to the control system. If the dual link is failed and this input is not received, this Microlok will lose ON_STANDBY status. This ensures that if the other side could possibly see that this side has failed, then this side cannot be online.

In the same way that the outputs drive independent relays, these inputs are not shared between the two masters.

An example of the interface circuits is shown in Appendix A of the engineering standard **Design of Microlok II Interlockings**.

Typical data for the THIS_MLK_OK functions is shown in section 6.3.1 of these **Dual Hot Standby Arrangements**.

6. Hot Standby Logic

6.2 Configuration, User Input and Version

To provide a confirmation that the correct data has been loaded into the Microlok, the CONFIGURATION block is used to require staff to enter details relating to the location and application logic revision. The entered values are saved in the EEPROM on the CPU backplane connector.

```
USER NUMERIC
ADDRESS_NUMBER :              "Set Location Address Number" ;
REVISION_NUMBER :             "Set Revision Number" ;
EXECUTIVE_VERSION:            "Set Executive Version Number" ;
```

The NUMERIC block at the end of the application logic tests the entered values, and if they do not match the values coded in the data, the KILLZ bit is set, which will in turn set KILL and reset the processor. The revision number is also converted to a set of bits to be passed over the dual link,and if the two processors are running different revisions of the application logic, the second processor to boot will be reset.

```
NUMERIC BEGIN

//PROGRAM VERIFICATION LOGIC

BLOCK 1 TRIGGERS ON CPS.ENABLE AND STALE AFTER 0:SEC;

//Convert the decimal "Version" number to a binary number
//Note_ Additional statements are required should the version number be greater than 15.

     IF ((REVISION_NUMBER/1 % 2) = 1) THEN ASSIGN TRUE TO VERSION_BIT1;
     END IF
     IF ((REVISION_NUMBER/2 % 2) = 1) THEN ASSIGN TRUE TO VERSION_BIT2;
     END IF
     IF ((REVISION_NUMBER/4 % 2) = 1) THEN ASSIGN TRUE TO VERSION_BIT3;
     END IF
     IF ((REVISION_NUMBER/8 % 2) = 1) THEN ASSIGN TRUE TO VERSION_BIT4;
     END IF

ASSIGN (ADDRESS_NUMBER <> 1) OR (REVISION_NUMBER <> 8) OR (EXECUTIVE_VERSION <> 510) TO KILLZ;

END BLOCK
END NUMERIC
```

6.2 Hot Standby Bits passed between Masters

The A_MASTER_ONLINE and A_ON_STANDBY bits are sent to the other interlocking master, and the B_MASTER_ONLINE and B_ON_STANDBY bits are received from the other interlocking master. In split masters, BOOT_UP is also sent to the other master, and B_BOOT_UP is received from the other master.

VERSION_BIT1, VERSION_BIT2, VERSION_BIT3, and VERSION_BIT4, are sent to the other interlocking master. I2_VERSION_BIT1, I2_VERSION_BIT2, I2_VERSION_BIT3, and I2_VERSION_BIT4, are received from the other interlocking master.

6.3 Only One Master

When a hot standby installation is working normally, one of the Microloks is the master on-line. This Microlok passes the controls across to the other Microlok via the dual link. Both Microloks then process the controls and then the results are compared via the dual links before the issue of controls to each data link.

As long as the dual link is functional the two interlockings are guaranteed to remain synchronised, or in the event that for any reason they differ, a control cannot be sent to the data link unless both interlockings agree.

In the event that a dual link fails there are two possible scenarios:

1. Only the Dual Link has failed
2. The other master has failed.

In the first scenario, there is a possibility that both masters could issue conflicting controls to the slaves. To prevent this, one must be forced off standby.

In the second scenario, there is no chance of conflicting controls being issued to the slave Microloks, as only one Microlok master is functional. Within this situation there are two possible actions:

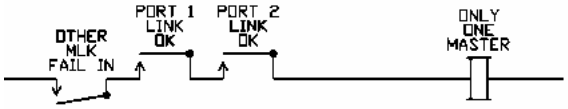
If the remaining Microlok is the on-line master, no further action is required as that Microlok can continue functioning and issuing controls to the slave Microloks.

If the remaining Microlok is on standby, then it can achieve Master on-line status. This is obtained by receiving an indication independent of the dual link that the other Microlok master has failed, and permitting the on-standby Microlok to achieve on-line status.

To achieve these requirements, an indication is required independent of the dual link. It is called ONLY_ONE_MASTER.

For interlockings with no slaves, or interlockings with duplicated slaves, a physical input OTHER_MLK_FAIL_IN is used in ONLY_ONE_MASTER:

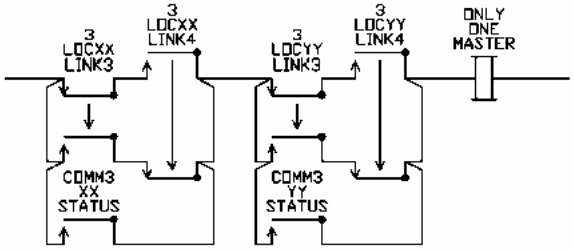
```
ASSIGN        OTHER_MLK_FAIL_IN * ~PORT2_LINK_OK * ~PORT1_LINK_OK                    TO ONLY_ONE_MASTER;
```



This input is derived from the THIS_MLK_OK_OUT of the other side as described in 6.3.1.

Where non-split masters control non-duplicated slaves, the slaves detect the status of the masters based solely on the status of the serial links to the masters, and return the status of both links to both masters. Each master can then determine if the other is still functioning.

```
ASSIGN        ((3_LOCXX_LINK_3 ^ 3_LOCXX_LINK_4) + ~COMM3.XX.STATUS) *
              ((3_LOCYY_LINK_3 ^ 3_LOCYY_LINK_4) + ~COMM3.YY.STATUS) *
              ((3_LOCZZ_LINK_3 ^ 3_LOCZZ_LINK_4) + ~COMM3.ZZ.STATUS)                    TO ONLY_ONE_MASTER;
```



If the master is a split master arrangement, MP2 may still be communicating with the slaves but MP1 has shutdown. To provide ONLY_ONE_MASTER in this case, MP2 determines MP1 status on the basis of the Port 4 link to MP1. This status is sent to each slave, and is included in the link status bits each slave returns to both masters. The ONLY ONE MASTER logic for split masters is the same as that used by the non-split master.

In MP2:

```
ASSIGN        PORT4_LINK_OK                                TO LOCXX_MP1_STATUS, LOCYY_MP1_STATUS, LOCZZ_MP1_STATUS;
```

In the slave:

```
ASSIGN        3_MP1_STATUS                                                  TO 3_LINK_3_MP1, 4_LINK_3_MP1;
ASSIGN        4_MP1_STATUS                                                  TO 3_LINK_4_MP1, 4_LINK_4_MP1;
```

In split masters, the ONLY_ONE_MASTER logic is in MP2, and the bit is repeated to MP1.

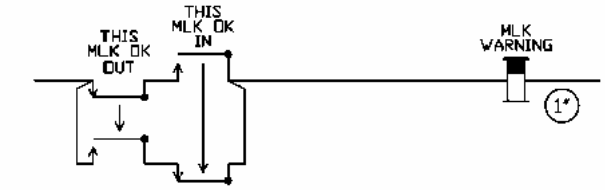
6.3.1 This Microlok OK

The Microlok OK bit forms part of the ONLY ONE MASTER logic of interlockings with either no slaves or duplicated slaves. It involves a relay interface between a pair of cardfiles which have vital output cards. The hardware interface is described in section 5.4.

```
ASSIGN        CPS.STATUS * A_ON_STANDBY                                     TO THIS_MLK_OK_OUT;
```

The relay is proved up in its own Microlok as THIS_MLK_OK_IN. This is to protect against the relay failing, which could result in a potentially unsafe indication to the other side. While the dual link is working, if THIS_MLK_OK_IN is not set, a warning is sent to the control system so staff can investigate the problem, but the Master can remain On Standby.

```
ASSIGN        THIS_MLK_OK_IN ^ THIS_MLK_OK_OUT                                TO MLK_WARNING;
```



If neither the THIS_MLK_OK_IN nor DUAL_LINK_OK bits are set, the master will lose A_ON_STANDBY. This ensures that if one side could be indicating failed when the dual link is failed, then that master is definitely not online. See the next section for this.

In split masters, the THIS_MLK_OK_OUT logic is in MP1, and the bit is repeated to MP2.

6.4 On Standby

Prior to an Interlocking Master being able to go online it must first achieve “On Standby” status, which demonstrates that the interlocking master is stand alone, or synchronised with the either interlocking master.

On initial boot up the “On Standby” status is achieved after:

- Proving the dual link (ports 1 & 2) to the other Interlocking Master are ok and following the boot up JR timing period.
- ONLY_ONE_MASTER bit is set, and the boot up JR timing period if the dual link is not operational.

If both Interlocking Masters are started together, both Interlocking Masters will achieve “On Standby” status at the same time if the dual link is ok.

Should a failure occur to the dual link when the interlocking master is already on standby, only the interlocking master that is on line will remain on standby (stick path). The DUAL MASTER OK has been provided to maintain the stick path if an interlocking changeover is occurring at the time of a dual link failure.

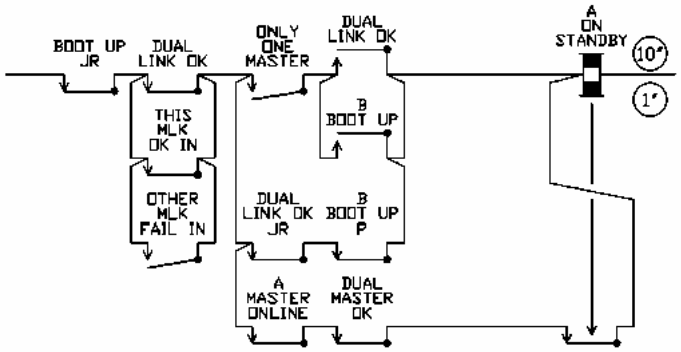
This function is slow to pick to allow time for any routes already set to be synchronised when “the other” RSR’s become set with the BOOT UP JR. It is inherently slow to drop due to the STALE DATA TIMEOUT. An additional release delay of 1 second is required in a split master configuration, which may be used in all configurations for consistency. It is needed because the link between MP1 and MP2 has been given a shorter STALE

DATA TIMEOUT than the dual link so that ONLY ONE MASTER can pick up sooner. With the STALE DATA time reduced, if the MASTER_ONLINE fails, the other master would lose A_ON_STANDBY before it received the CONTROL_SYSTEM_MASTER bit.

```
ADJUSTABLE A_ON_STANDBY:        SET=10:SEC    CLEAR=1SEC;
```

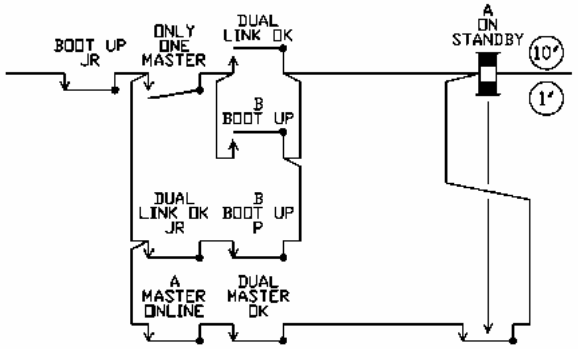
For interlocking masters with no slaves or duplicated slaves:

```
ASSIGN        BOOT_UP_JR * (DUAL_LINK_OK + THIS_MLK_OK_IN + OTHER_MLK_FAIL_IN) *
              ((ONLY_ONE_MASTER * (~DUAL_LINK_OK + ~B_BOOT_UP)) +
               (DUAL_LINK_OK_JR * B_BOOT_UP_P) +
               (A_MASTER_ONLINE * DUAL_MASTER_OK * A_ON_STANDBY))                    TO A_ON_STANDBY;
```



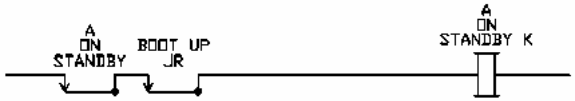
For interlocking masters with non-duplicated slaves:

```
ASSIGN        BOOT_UP_JR *
              ((ONLY_ONE_MASTER * (~DUAL_LINK_OK + ~B_BOOT_UP)) +
               (DUAL_LINK_OK_JR * B_BOOT_UP_P) +
               (A_MASTER_ONLINE * DUAL_MASTER_OK * A_ON_STANDBY))                    TO A_ON_STANDBY;
```



To maintain the quickest possible mastership change when the online master loses ON STANDBY, the indication bit sent to the control system takes BOOT UP JR in series with ON STANDBY.

```
ASSIGN        BOOT_UP_JR * A_ON_STANDBY                                             TO A_ON_STANDBY_K;
```



6.5 Master Online

The Control System will determine which of the two Interlocking masters is to go “Online”. The primary purpose of the MASTER_ONLINE bit is to ensure that in the event of a failure affecting synchronisation, the control system continues to communicate with the functioning master.

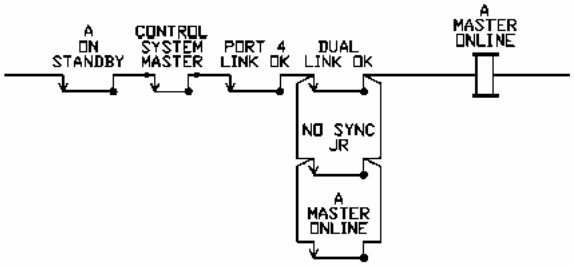
The Control system link must be established via the serial port status logic (PORT_4_LINK_OK) bit before an Interlocking Master can go “Online”, ensuring recent controls have been received when the link is first established.

With the link to the Control System proven ok and the Interlocking Master already “On Standby”, the Control System will send the data bit “Control System Master” to the Interlocking Master and that interlocking will go “Online”.

If the dual link is failed at the time of the Interlocking Master receiving the “control system master” bit from the Control System, that Interlocking Master cannot become the “Online” Master until after the NO_SYNC_JR timing period.

A MASTER ON LINE - An interlocking master may achieve on line status if already on standby and once the control system sends the control system master bit. The link to the control system is proven to guard against the possibility of frozen bits in the Genisys link. If the dual link is not ok, on line status cannot be achieved until the No Sync JR timing period.

```
ASSIGN        A_ON_STANDBY * CTR_SYS_MASTER * PORT_4_LINK_OK *
              (DUAL_LINK_OK + NO_SYNC_JR + A_MASTER_ONLINE)                TO A_MASTER_ONLINE;
```




```
NV.ASSIGN     A_MASTER_ONLINE                                             TO A_MASTER_ONLINEK;
```

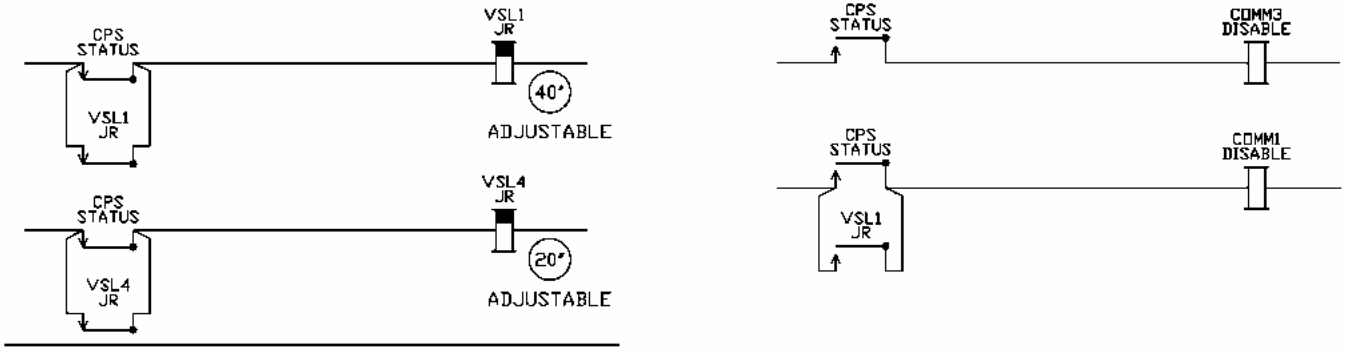
6.6 Serial Port Control Logic

Vital serial links are to be disabled if CPS.STATUS is down.

In order to prevent the Microlok repeatedly rebooting because too many bits change during start-up, timers are used to stagger the initialisation of serial links.

```
ADJUSTABLE VSL1JR: SET=40:SEC    CLEAR=0:SEC;
ADJUSTABLE VSL4JR: SET=20:SEC    CLEAR=0:SEC;

     ASSIGN        ~CPS.STATUS                                             TO COMM3.DISABLE;
     ASSIGN        ~CPS.STATUS + ~VSL1JR                                   TO COMM1.DISABLE;
     ASSIGN        ~CPS.STATUS + ~VSL1JR                                   TO COMM2.DISABLE;
     ASSIGN        ~CPS.STATUS + ~VSL4JR                                   TO COMM4.DISABLE;
     ASSIGN        CPS.ENABLE + VSL1JR                                     TO VSL1JR;
     ASSIGN        CPS.ENABLE + VSL4JR                                     TO VSL4JR;
```

VSL1JR is used a common timer for both port 1 and port2 (the dual link). There is no delay in initialising the link to the slaves.



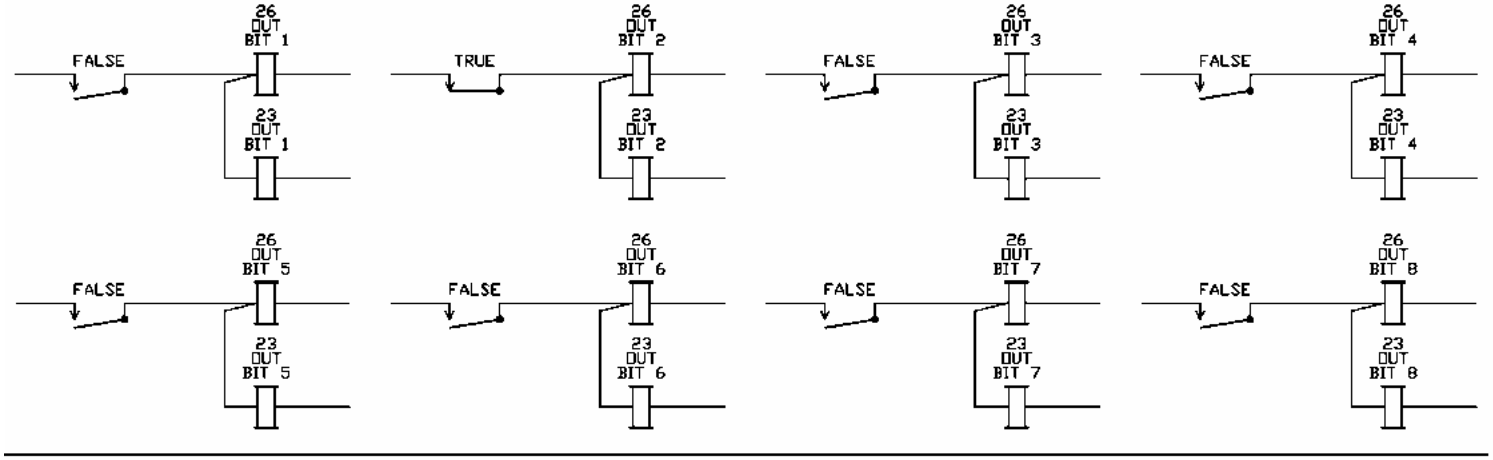
6.7 Interlocking Addressing

In addition to the addresses used on the vital links between masters and slaves, each interlocking is to be allocated a unique address. The address number is to be sent as the first 8 bits of information in the communication data between cardfiles. The received interlocking address is to be verified before the data is permitted to be processed. This occurs both ways between masters and slaves.

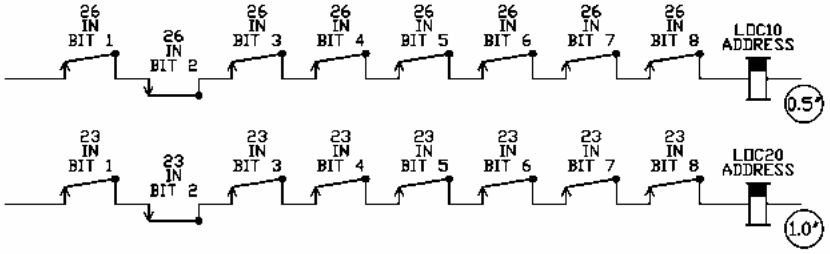
The LOCxx_ADDRESS bits in the master are also used to spread the load of bits changing simultaneously during link startup. In the master, each LOCxx.ADDRESS bit is delayed by a different amount, in increments of 500ms. This prevents the repeat bits in the masters changing all at once.

In the master,

```
ADJUSTABLE LOC10_ADDRESS: SET=500:MSEC    CLEAR=0:SEC;
ADJUSTABLE LOC20_ADDRESS: SET=1000:MSEC   CLEAR=0:SEC;

     ASSIGN        FALSE                                                    TO 26_OUT_BIT1, 23_OUT_BIT1;
     ASSIGN        TRUE                                                     TO 26_OUT_BIT2, 23_OUT_BIT2;
     ASSIGN        FALSE                                                    TO 26_OUT_BIT3, 23_OUT_BIT3;
     ASSIGN        FALSE                                                    TO 26_OUT_BIT4, 23_OUT_BIT4;
     ASSIGN        FALSE                                                    TO 26_OUT_BIT5, 23_OUT_BIT5;
     ASSIGN        FALSE                                                    TO 26_OUT_BIT6, 23_OUT_BIT6;
     ASSIGN        FALSE                                                    TO 26_OUT_BIT7, 23_OUT_BIT7;
     ASSIGN        FALSE                                                    TO 26_OUT_BIT8, 23_OUT_BIT8;
```

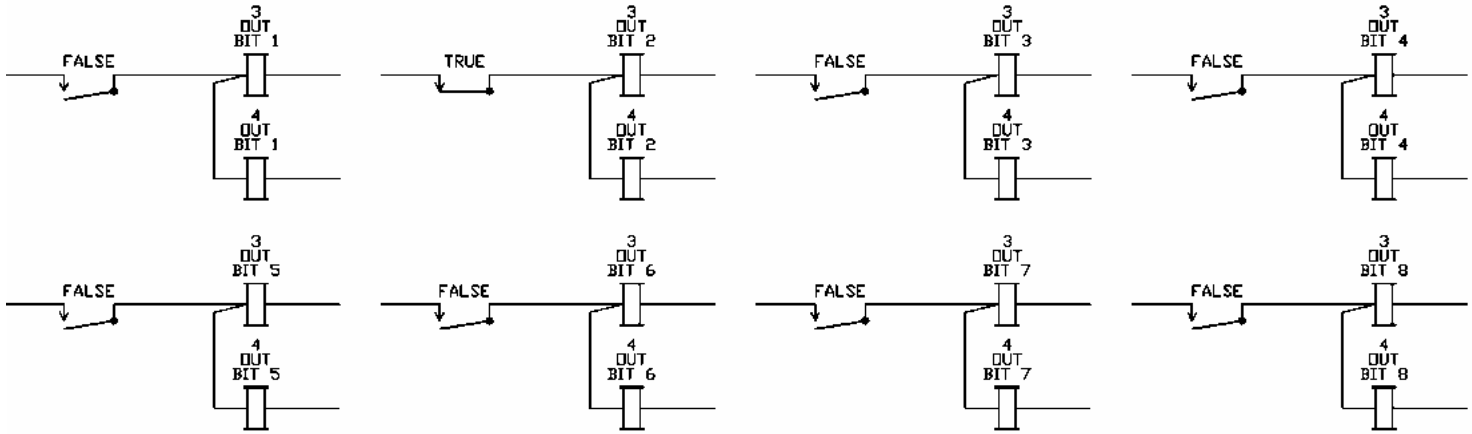



```
ASSIGN          ~26_IN_BIT1 * 26_IN_BIT2 * ~26_IN_BIT3 * ~26_IN_BIT4 *
                ~26_IN_BIT5 * ~26_IN_BIT6 * ~26_IN_BIT7 * ~26_IN_BIT8          TO LOC10_ADDRESS;

ASSIGN          ~23_IN_BIT1 * 23_IN_BIT2 * ~23_IN_BIT3 * ~23_IN_BIT4 *
                ~23_IN_BIT5 * ~23_IN_BIT6 * ~23_IN_BIT7 * ~23_IN_BIT8          TO LOC20_ADDRESS;
```

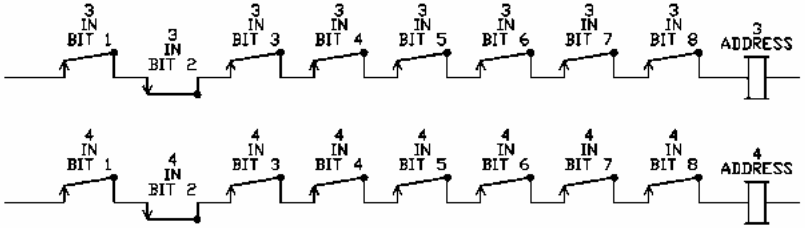


In non-duplicated slaves.

```
ASSIGN          FALSE                                                   TO 3_OUT_BIT1, 4_OUT_BIT1;
ASSIGN          TRUE                                                    TO 3_OUT_BIT2, 4_OUT_BIT2;
ASSIGN          FALSE                                                   TO 3_OUT_BIT3, 4_OUT_BIT3;
ASSIGN          FALSE                                                   TO 3_OUT_BIT4, 4_OUT_BIT4;
ASSIGN          FALSE                                                   TO 3_OUT_BIT5, 4_OUT_BIT5;
ASSIGN          FALSE                                                   TO 3_OUT_BIT6, 4_OUT_BIT6;
ASSIGN          FALSE                                                   TO 3_OUT_BIT7, 4_OUT_BIT7;
ASSIGN          FALSE                                                   TO 3_OUT_BIT8, 4_OUT_BIT8;
```




```
ASSIGN          ~26_IN_BIT1 * 26_IN_BIT2 * ~26_IN_BIT3 * ~26_IN_BIT4 *
                ~26_IN_BIT5 * ~26_IN_BIT6 * ~26_IN_BIT7 * ~26_IN_BIT8   TO 3_ADDRESS;

ASSIGN          ~23_IN_BIT1 * 23_IN_BIT2 * ~23_IN_BIT3 * ~23_IN_BIT4 *
                ~23_IN_BIT5 * ~23_IN_BIT6 * ~23_IN_BIT7 * ~23_IN_BIT8   TO 4_ADDRESS;
```



Duplicated slaves only need addressing logic for port 3.

6.8 Serial Port Status logic

Microlok II communications links can use either the vital Microlok or non-vital Genisys protocol. Each protocol allows multiple "station addresses" to be defined on the link, allowing one master to communicate with many slaves. There is a limit to how many bits can be sent each way under one address: 128 for a vital link, and 512 for a non-vital. Where more bits must be sent, two or more addresses can be used at one location. Each address on a link has its own STATUS bit, and all status bits for a link can be combined to determine the status of the entire link.

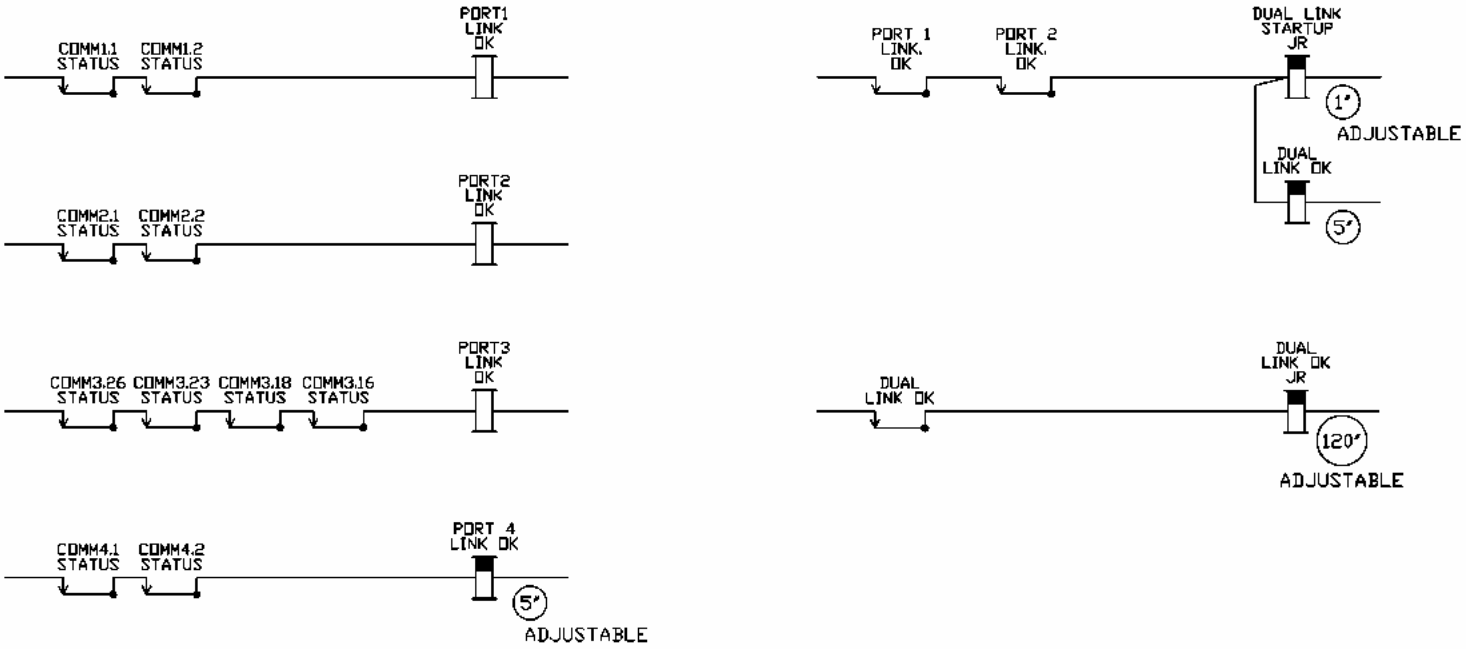
PORT 4 LINK OK - Proves the connection to the Control System is made. The 5-second slow to set timer ensures the link is stable and controls are up-to-date before they are accepted. This function is especially important as bits on the non-vital link freeze in their last state when the link fails. PORT4_LINK_OK is used to prevent controls holding up when the link fails.

DUAL LINK OK - Proves the links between the two interlocking masters is ok. The 5-second slow to set timer is provided to ensure bits have been set to the correct state before the link is accepted as operational.

DUAL LINK OK JR – This timer is provided to allow time for a "warm re-sync". If the dual link has failed, the interlocking which is not MASTER ONLINE will lose A_ON_STANDBY. When the dual link is restored, BOOT_UP_JR is already up, but some timers may not be synchronised. DUAL_LINK_OK_JR will prevent this master regaining A_ON_STANDBY until time has passed to allow re-synchronisation.

For non-split interlocking masters:

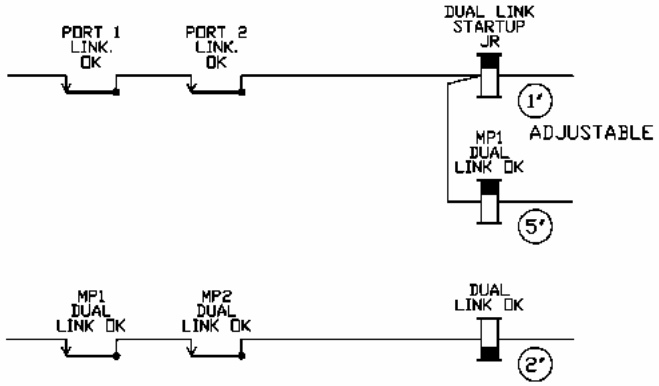
```
DUAL_LINK_STARTUP_JR:       SET=1:SEC         CLEAR=0:SEC
DUAL_LINK_OK:               SET=5:SEC         CLEAR=0:SEC;
DUAL_LINK_OK_JR:            SET=120:SEC       CLEAR=0:SEC;
PORT4_LINK_OK:              SET=5:SEC         CLEAR=0:SEC;

ASSIGN        COMM1.1.STATUS * COMM1.2.STATUS                                                    TO PORT1_LINK_OK;
ASSIGN        COMM2.1.STATUS * COMM2.2.STATUS                                                    TO PORT2_LINK_OK;
ASSIGN        COMM3.26.STATUS * COMM3.23.STATUS * COMM3.18.STATUS * COMM3.16.STATUS              TO PORT3_LINK_OK;
ASSIGN        COMM4.1.STATUS * COMM4.2.STATUS                                                    TO PORT4_LINK_OK;
ASSIGN        PORT2_LINK_OK * PORT1_LINK_OK                                TO DUAL_LINK_STARTUP_JR, DUAL_LINK_OK;
ASSIGN        DUAL_LINK_OK                                                                  TO DUAL_LINK_OK_JR;
```



For split interlocking masters:

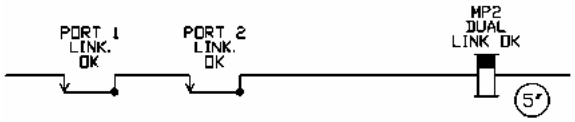
In Interlocking 1

```
MP1_DUAL_LINK_OK:        SET=5:SEC          CLEAR=0:SEC;
DUAL_LINK_OK:            SET=0:SEC          CLEAR=2:SEC;

ASSIGN        PORT2_LINK_OK * PORT1_LINK_OK                    TO DUAL_LINK_STARTUP_JR, MP1_DUAL_LINK_OK;
ASSIGN        MP1_DUAL_LINK_OK * MP2_DUAL_LINK_OK                              TO DUAL_LINK_OK;
```



In Interlocking 2

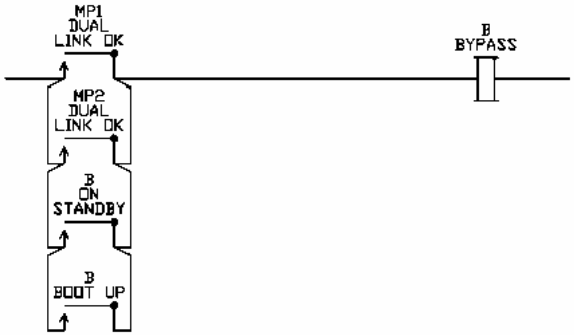
```
MP2_DUAL_LINK_OK:        SET=5:SEC            CLEAR=0:SEC;

ASSIGN          PORT2_LINK_OK * PORT1_LINK_OK                                    TO MP2_DUAL_LINK_OK;
```



6.9 Bypass logic

B BYPASS - Used to qualify the output bit comparison, when the dual link has failed and the status of the other interlocking master is unknown or when the other interlocking master is not on standby.

```
ASSIGN          ~MP1_DUAL_LINK_OK + ~MP2_DUAL_LINK_OK + ~B_ON_STANDBY + B_BOOT_UP                TO B_BYPASS;
```



For split interlocking masters include in Interlocking 2:

```
ASSIGN          I4_B_BYPASS + ~MP2_DUAL_LINK_OK                                  TO B_BYPASS;
```

6.10 Startup and Synchronisation logic

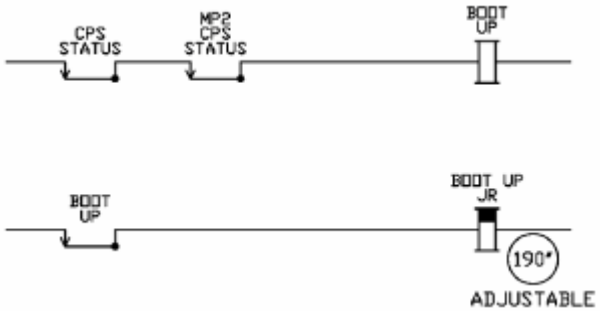
BOOT UP JR - Starts to time when the application initially starts up, provides time for the interlocking masters to become synchronised. The slow to set time delay (nominally 190 seconds) is set based on it being 10 seconds longer than the longest locking timer (ALSJR or USR track timer) plus any delay in establishing the dual link.

For single interlocking masters:

```
ADJUSTABLE BOOT_UP_JR:        SET=190:SEC          CLEAR=0:SEC;
           FLASH:             SET=500:MSEC         CLEAR=500:MSEC;

     ASSIGN        CPS.STATUS                                                    TO BOOT_UP;
```

For split interlocking masters use the following logic in Interlocking 1:

```
ASSIGN          CPS.STATUS * 3_MP2_CPS.STATUS                                   TO BOOT_UP;

ASSIGN          BOOT_UP                                                         TO BOOT_UP_JR;
```

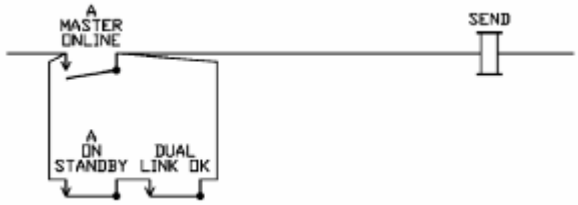


Indicate boot up status by flashing LED 8.

```
NV.ASSIGN       BOOT_UP_JR * (~NO_SYNC_R + NO_SYNC_JR) +
                (BOOT_UP * ~BOOT_UP_JR + NO_SYNC_R * ~NO_SYNC_JR) * FLASH       TO LED.8;
```

SEND - Outputs from the interlocking masters cannot be sent unless this interlocking master is actually the master on line or the dual link is ok and this interlocking master has ON_STANDBY status.

```
ASSIGN          A_MASTER_ONLINE + (DUAL_LINK_OK * A_ON_STANDBY)                 TO SEND;
```

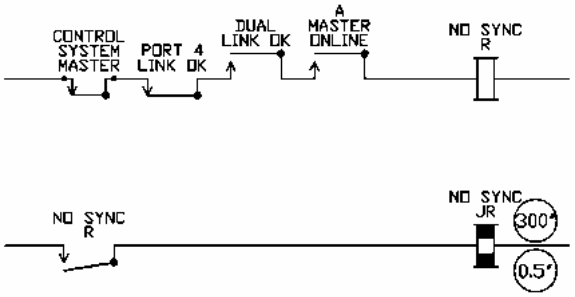


In Interlocking 2

```
ASSIGN          4_SEND                                                          TO SEND;
```

NO SYNC JR - Should an interlocking master be called to go online when the dual link has failed, that interlocking must wait for until all signals have timed out and any trains have come to a stand, as the state of the other Master interlocking (including any routes set) is unknown. A 300-second slow to set timing period is assumed to satisfy this requirement as it includes the 120 second approach linking timeout, and a 180 second running time to the next signal. Again the Genisys link is proven ok to guard against frozen bits in the link. Note the timing period does not start until the control system master bit is received.

```
ADJUSTABLE NO_SYNC_JR:   SET=300:SEC    CLEAR=500:MSEC;
     ASSIGN         CTR_SYS_MASTER * PORT_4_LINK_OK * ~DUAL_LINK_OK * ~A_MASTER_ONLINE                TO NO_SYNC_R;
     ASSIGN         NO_SYNC_R                                                                         TO NO_SYNC_JR;
```



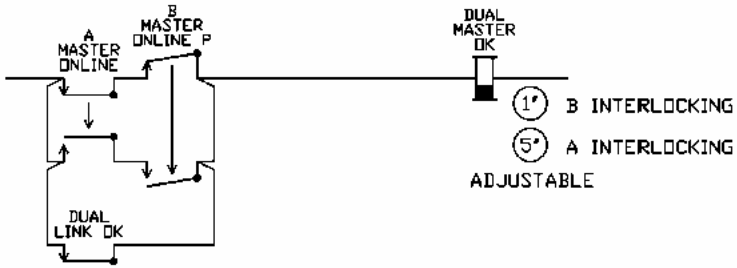
B MASTER ON LINE P - This is a direct repeat function of B MASTER ON LINE and is 3-seconds slow to drop. It is used in the DUAL_MASTER_OK logic.

```
ADJUSTABLE B_MASTER_ONLINE_P:   SET=0:SEC    CLEAR=3:SEC;
     ASSIGN         B_MASTER_ONLINE                                                                   TO B_MASTER_ONLINE_P;
```

DUAL MASTER OK - This is used in the stick path of the A ON STANDBY statement and allows the on standby status to be maintained should both interlocking masters be on line at the time of a dual link failure. The 1st and 2nd paths are broken when both interlockings are online. The slow to clear time delay is set in conjunction with B_MASTER_ONLINE_P to bias the system to the A interlocking master remaining online. The A system is set as 5 seconds slow to clear, and the B system is set as 1 second slow to clear.

The A interlocking DUAL_MASTER_OK will be slower to drop away than the B interlocking, as set through the adjustable timers, and will hold as the B_MASTER_ON_LINE_P drops between the A and B times to leave the A interlocking online in this case.

```
ADJUSTABLE DUAL_MASTER_OK:      SET=0:SEC    CLEAR=1:SEC; // THIS TIMER MUST BE SET TO 5 SEC FOR THE "A' INTERLOCKING
     ASSIGN         (A_MASTER_ONLINE ^ B_MASTER_ONLINE_P) + DUAL_LINK_OK                              TO DUAL_MASTER_OK;
```



6.11 Synchronisation of Interlocking

In order to ensure either Interlocking Master is capable of going online and assuming control of the interlocking it is essential that both Interlocking Masters remain in synchronisation with each other.

Synchronisation requires consideration of:

- The external equipment status input into the slaves
- The controls received from the Control System
- The internal logic states, which may not directly relate to the current input states
- Outputs sent to the interlocking slaves
- Startup conditions, and hot standby status

The synchronisation is achieved by passing via the dual link (ports 1 & 2) all input bits from the slave locations, the control bits, and all output bits to the slave locations.

All input bits from the slave locations are OR'd with the input bits from the other side. This excludes all input bits required by the Control System for health calculation arbitration. The timing considerations are Delay in detection as OFF can be one extra cycle time delay, or one Stale Data Timeout. Minimum duration to be detected as OFF no change when system operating correctly, it remains as one Stale Data Timeout during failure case.

The control bits are OR'd with the control bits from the other side after consideration of the Hot Standby status. The timing considerations are the duration a control bit must be held ON to ensure it is set in the other side via the dual link. If control bits are to be latched in the Interlocking master to handle short duration or pulsed controls then there must be a method to latch them in the other interlocking master during startup.

All output bits to the slave locations are AND'd with the output bits from the other side after consideration of the Hot Standby status. Output comparison timing issues are:

- Outputs turning OFF – comparison has no impact because they are AND'd, however due to timing when polling slaves the output could be delayed by one slave cycle time in turning OFF.
- Outputs turning ON – comparison has an impact because they are AND'd, and the maximum extra delay is twice the dual link cycle time.

Ensuring the outputs of both Interlocking Masters are compared prior to the outputs being sent to the slave locations proves output synchronisation.

Failure of the dual link (ports 1 or 2) or if the "B" or "other" Interlocking Master has failed or is not on standby will result in the "A" or "this" Interlocking Master ignoring all the synchronisation output bits of the other Interlocking Master.

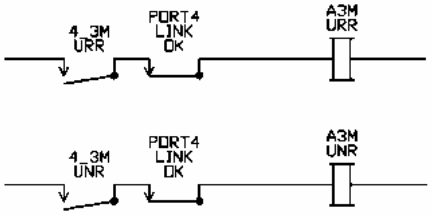
Failure of a dual link (ports 1 or 2) will also result in no outputs being sent by the Interlocking Master that is not online. Should a failure then occur with the online Interlocking Master, signals will normalise until switching by the Control System occurs.

Synchronisation of Route and Points Calls

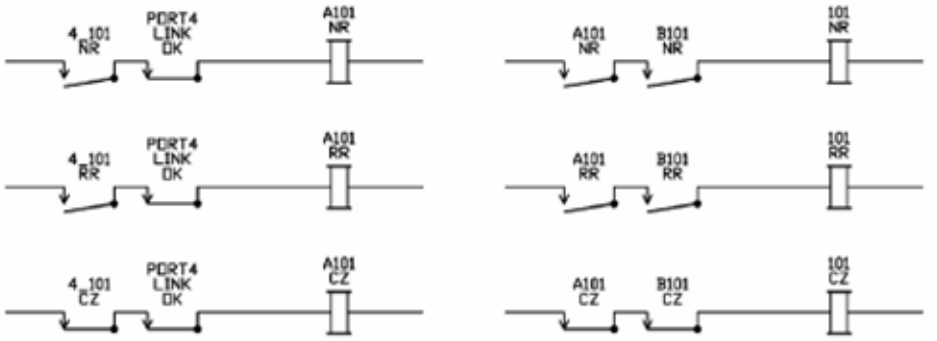
Only those functions which are changed by Hot Standby are shown here. All other signal and points functions are as shown in section 4.5 of the specification Design of Microlok II Interlockings.

Control System: Request bits from the control system are sent to both masters. With the exception of URR bits and the CONTROL_SYSTEM_MASTER bit, the request bits are passed across the dual link after ensuring the control system link is ok. This allows both masters to process requests and remain fully synchronised even if the control system link to one master fails. The URR bit is not passed across the link, the A_(ROUTE)_RSR is passed instead.

```
ASSIGN        4_3M_URR * PORT_4_LINK_OK                          TO A3M_URR;
ASSIGN        4_3M_UNR * PORT_4_LINK_OK                          TO A3M_UNR;
```



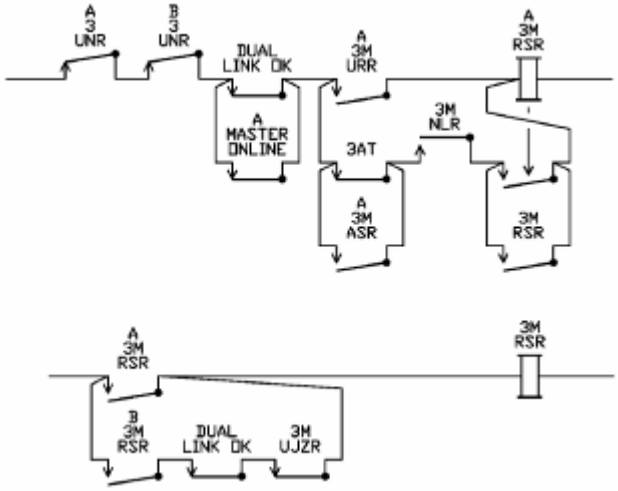

```
ASSIGN        4_101_CZ * PORT_4_LINK_OK                          TO A101_CZ;
ASSIGN        4_101_NR * PORT_4_LINK_OK                          TO A101_NR;
ASSIGN        4_101_RR * PORT_4_LINK_OK                          TO A101_RR;
ASSIGN        A101_CZ + B101_CZ                                   TO 101_CZ;
ASSIGN        A101_NR + B101_NR                                   TO 101_NR;
ASSIGN        A101_RR + B101_RR                                   TO 101_RR;
```



RSR: the A_(ROUTE)_RSR responds directly to the control system route request URR. The A_(ROUTE)_RSR bit is passed across the dual link, and received on the other side as B_(ROUTE)_RSR. The two are combined into the (ROUTE)_RSR. This ensures that routes already set in the ONLINE master are correctly set in the other master if it has just rebooted.

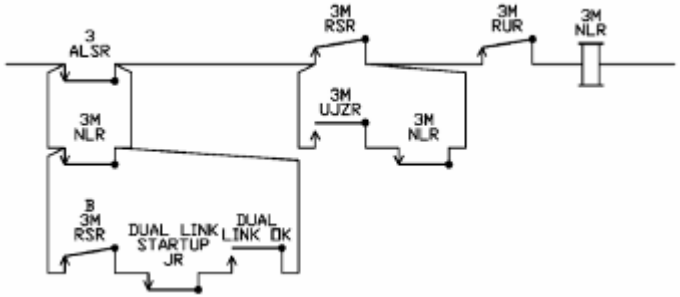
The control system route normalising request UNR is passed across the dual link without any additional processing. Either the A_(ROUTE)_UNR or B_(ROUTE)_UNR will be effective to cancel the route.

```
ASSIGN      ~A3_UNR * ~B3_UNR * (DUAL_LINK_OK + A_MASTER_ONLINE) *
            (A3M_URR + ((3AT + 3_ASR) * ~3M_NLR * (A3M_RST + 3M_RSR)))      TO A3M_RSR;
ASSIGN      A3M_RSR + B3M_RSR * DUAL_LINK_OK * 3M_UJZR                       TO 3M_RSR;
```



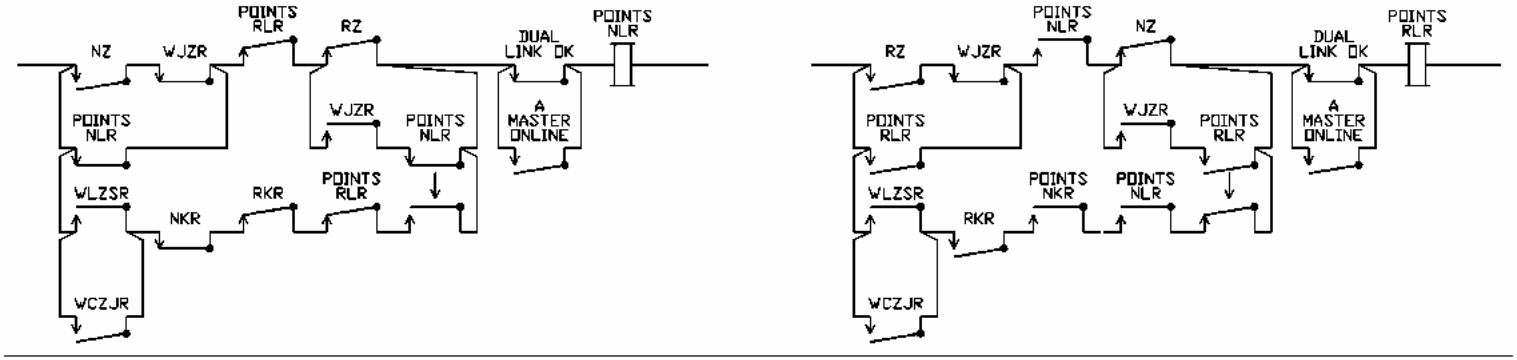
Route NLR: If one route on a multi-route signal is set when a master recovers after a reboot, the ALSR will be down. The B_(ROUTE)_RSR down is provided to pick up the corresponding NLR during dual link restoration, in the 4 second window between DUAL_LINK_STARTUP_JR and DUAL_LINK_OK picking.

```
ASSIGN          (3ALSR + 3M_NLR + ~B3M_RSR * DUAL_LINK_STARTUP_JR * ~DUAL_LINK_OK) *
                (~3M_RSR + ~3M_UJZR * 3M_NLR) * ~3M_RUR_                          TO 3M_NLR;
```



Points NLR, RLR: DUAL_LINK_OK + A_MASTER_ONLINE is included in series in the NLR and RLR logic to drop out these bits if the dual link fails and this master is not online. Combined with the DUAL_LINK_OK_JR and the WLZSR, this allows the points lock relays to synchronise with the points detection when the master recovers from the dual link failure.

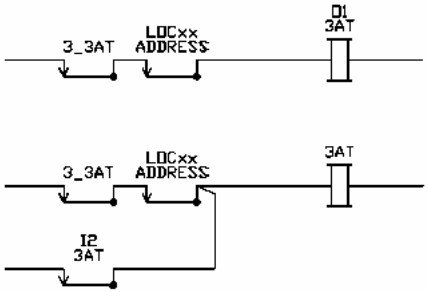
```
ASSIGN          (((101_NZ * 101WJZR + 101_NLR) * ~101_RLR * (~101_RZ + ~101WJZR * 101_NLR) +
                (~101_WLZSR + 101_WCZJR) * 101_NKR * ~101_RKR * ~101_RLR * ~101_NLR)) *
                (DUAL_LINK_OK + A_MASTER_ONLINE)                                  TO 101_NLR;

ASSIGN          (((101_RZ * 101WJZR + 101_RLR) * ~101_NLR * (~101_NZ + ~101WJZR * 101_RLR) +
                (~101_WLZSR + 101_WCZJR) * 101_RKR * ~101_NKR * ~101_RLR * ~101_NLR)) *
                (DUAL_LINK_OK + A_MASTER_ONLINE)                                  TO 101_RLR;
```



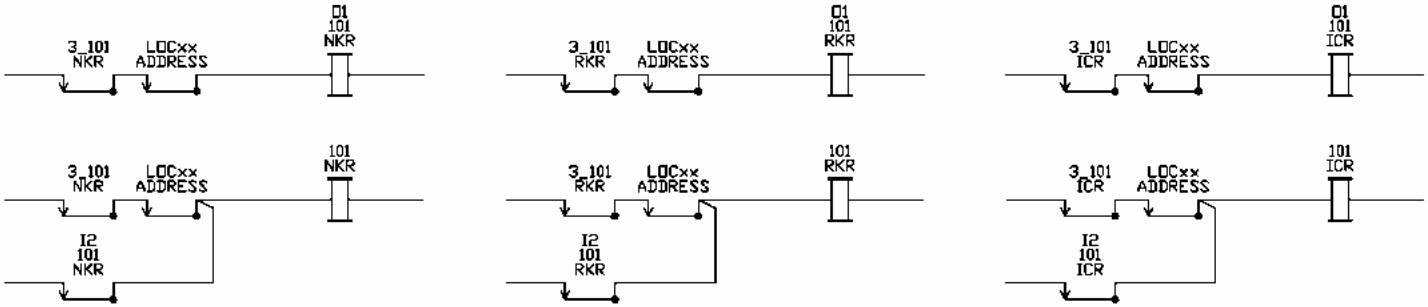
Synchronisation of Field Inputs

Inputs from the field equipment, including track circuits, trainstop and points detection, and signal control relay proving, are shared across the dual link, to ensure that both interlockings can remain synchronised even if the link between one master and the slaves fails.

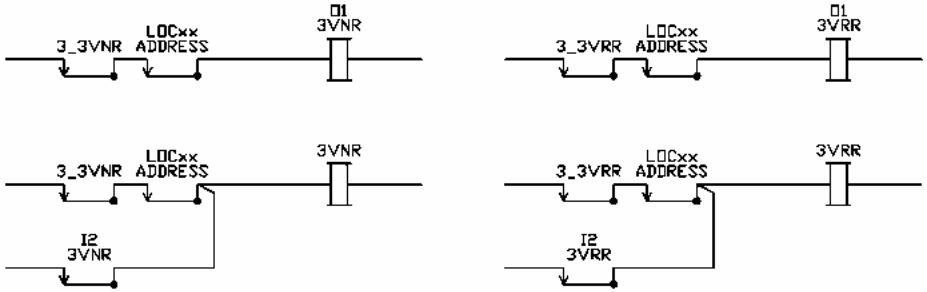
```
ASSIGN        3_3AT * LOCxx_ADDRESS                          TO O1_3AT;
ASSIGN        3_3AT * LOCxx_ADDRESS + i2_3AT                 TO 3AT
```




```
ASSIGN        3_101NKR * LOCxx_ADDRESS                       TO O1_101NKR;
ASSIGN        3_101RKR * LOCxx_ADDRESS                       TO O1_101RKR;
ASSIGN        3_101ICR * LOCxx_ADDRESS                       TO O1_101ICR;
ASSIGN        3_101NKR * LOCxx_ADDRESS + I2_101NKR           TO 101NKR;
ASSIGN        3_101RKR * LOCxx_ADDRESS + I2_101RKR           TO 101RKR;
ASSIGN        3_101ICR * LOCxx_ADDRESS + I2_101ICR           TO 101ICR;
```




```
ASSIGN      3_3VNR * LOCxx_ADDRESS                          TO 01_3VNR;
ASSIGN      3_3VRR * LOCxx_ADDRESS                          TO 01_3VRR;
ASSIGN      3_3VNR * LOCxx ADDRESS + I2_3VNR                TO 3VNR;
ASSIGN      3_3VRR * LOCxx_ADDRESS + I2_3VRR                TO 3VRR;
```

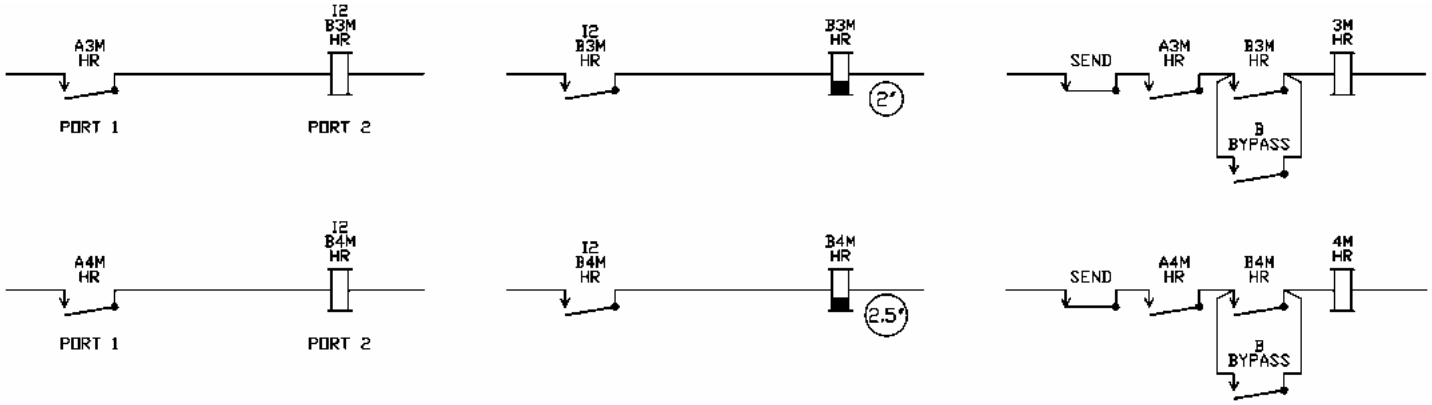


Comparison of Interlocking Outputs

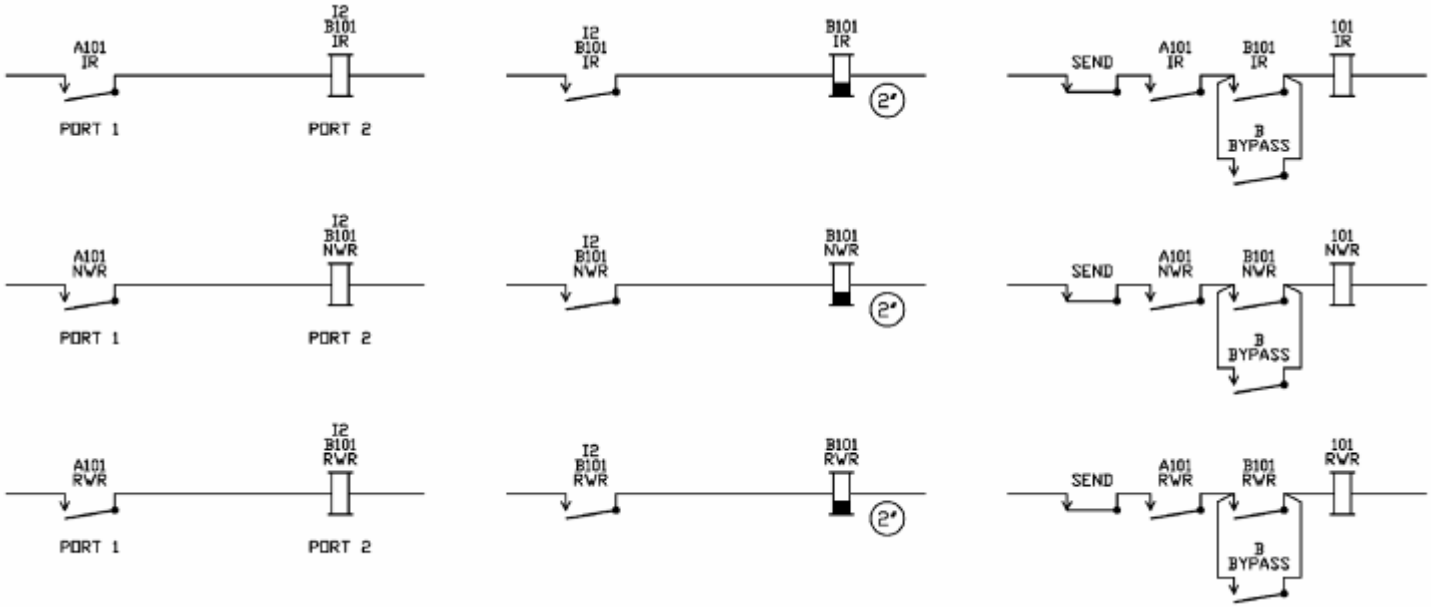
Interlocking control functions, such as signal and points controls, are independently processed to an intermediate stage by each master. This intermediate bit is denoted by the prefix “A”. Before being sent to the slaves, the outputs of both interlocking masters are compared, and both masters must agree in order for set bits to be sent to the slaves. The “A” bits are passed across the dual link, and received as “B” bits. In the event of a failure, the B_BYPASS will be set in the MASTER ONLINE, enabling the MASTER ONLINE to send outputs to the slaves without performing the comparison. The “B” bits from the other master are given a slow release repeat to allow time for B BYPASS to pick up. In general this delay is set to 2 seconds, but for up signals it is made 2.5 seconds to prevent the Microlok error “Too many bits changed at once”.

In a split master system, the data is processed to the intermediate stage in MP1, then the bits are passed to MP2. Output comparison processed in MP2.

```
ADJUSTABLE B3M_HR:       SET=0:SEC      CLEAR=2:SEC;
ADJUSTABLE B4M_HR:       SET=0:SEC      CLEAR=2500:MSEC;
ADJUSTABLE B101_NWR:     SET=0:SEC      CLEAR=2:SEC;
ADJUSTABLE B101_RWR:     SET=0:SEC      CLEAR=2:SEC;
ADJUSTABLE B101_IR:      SET=0:SEC      CLEAR=2:SEC;

     ASSIGN         ~3M_USR * ~3BT_JRP *  ~3BT_JR *
                    ~3NGPR * ~3ALSR * ~3M_ALSJR * 3M_UCR                    TO A3M_HR;

     ASSIGN         I2_B3M_HR                                               TO B3M_HR;
     ASSIGN    SEND * A3M_HR * (B3M_HR + B_BYPASS)                          TO 3M_HR;
```




```
     ASSIGN         101_NLR                                                 TO A101_NWR:
     ASSIGN         101_RLR                                                 TO A101_RWR;
     ASSIGN         (101_NLR * ~101_NKR + 101_RLR * ~101_RKR) * ~101_WTJR * 101EOL *
                    (3AT * 7AT * 3ALSR + A101_IR)                           TO A101_IR;

     ASSIGN         I2_B101_NWR                                             TO B101_NWR;
     ASSIGN         I2_B101_RWR                                             TO B101_RWR;
     ASSIGN         I2_B101_IR                                              TO B101_IR;

     ASSIGN         SEND * A101_NWR * (B101_NWR + B_BYPASS)                 TO 101_NWR;
     ASSIGN         SEND * A101_RWR * (B101_RWR + B_BYPASS)                 TO 101_RWR;
     ASSIGN         SEND * A101_IR * (B101_IR * (B101_IR + B_BYPASS)        TO 101_IR;
```


A101
IR
I2
B101
IR
PORT 1
PORT 2
I2
B101
IR
B101
IR
2"
SEND
A101
IR
B101
IR
101
IR
B
BYPASS
A101
NWR
I2
B101
NWR
PORT 1
PORT 2
I2
B101
NWR
B101
NWR
2"
SEND
A101
NWR
B101
NWR
101
NWR
B
BYPASS
A101
RWR
I2
B101
RWR
PORT 1
PORT 2
I2
B101
RWR
B101
RWR
2"
SEND
A101
RWR
B101
RWR
101
RWR
B
BYPASS

Attachment A – Superseded Data Structures for NX-Style Interlocking

Earlier installations of Dual Hot Standby Microlok interlockings used NX-style route setting. In this arrangement, the NLR and RUR are directly operated by the momentary route call, and the RUR sticks with the commence button not pulled (FM)R. With no RSR or equivalent, synchronisation of the MASTER ONLINE and the other master is by passing the NLR and RUR bits across the dual link. With the A_BYPASS bit set in the master which is not ONLINE, the NLRs and RURs, and points NLRs and RLRs operate as direct repeats of the functions in the MASTER ONLINE.

Such interlockings are still in use, and when small modifications are needed, it may be appropriate to continue with the NX style rather than making large-scale changes to rewrite the application for OCS.

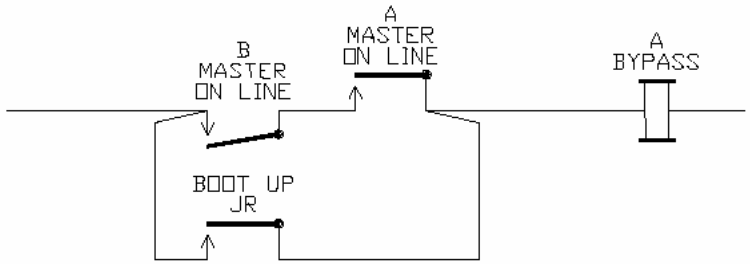
When working with installations using this methodology, staff should be aware that the bits in the master which is not online (and hence logs of those bits) may not give a true representation of the status of field equipment. For example, because control system bits are only received in the online master, points CZ bits are not set in the standby unit, and thus the WJZR bits will also be down. Because the synchronisation is achieved by NLRs and RLRs, the locking will still function correctly.

Apart from the use of the A_BYPASS function, the Hot Standby logic is conceptually the same as current standards, but there have been slight changes as the design has evolved. It is not possible to show all variants here, and for small interlocking changes it should not be necessary to modify the Hot Standby logic.

For larger interlocking changes, or where Hot Standby deficiencies need to be corrected, consideration should be given to migrating to the OCS logic.

A BYPASS – Provides forced synchronisation to the interlocking master that is not the master on line. The locking functions of the interlocking master that is not on line will work as a repeat of the master that is on line.

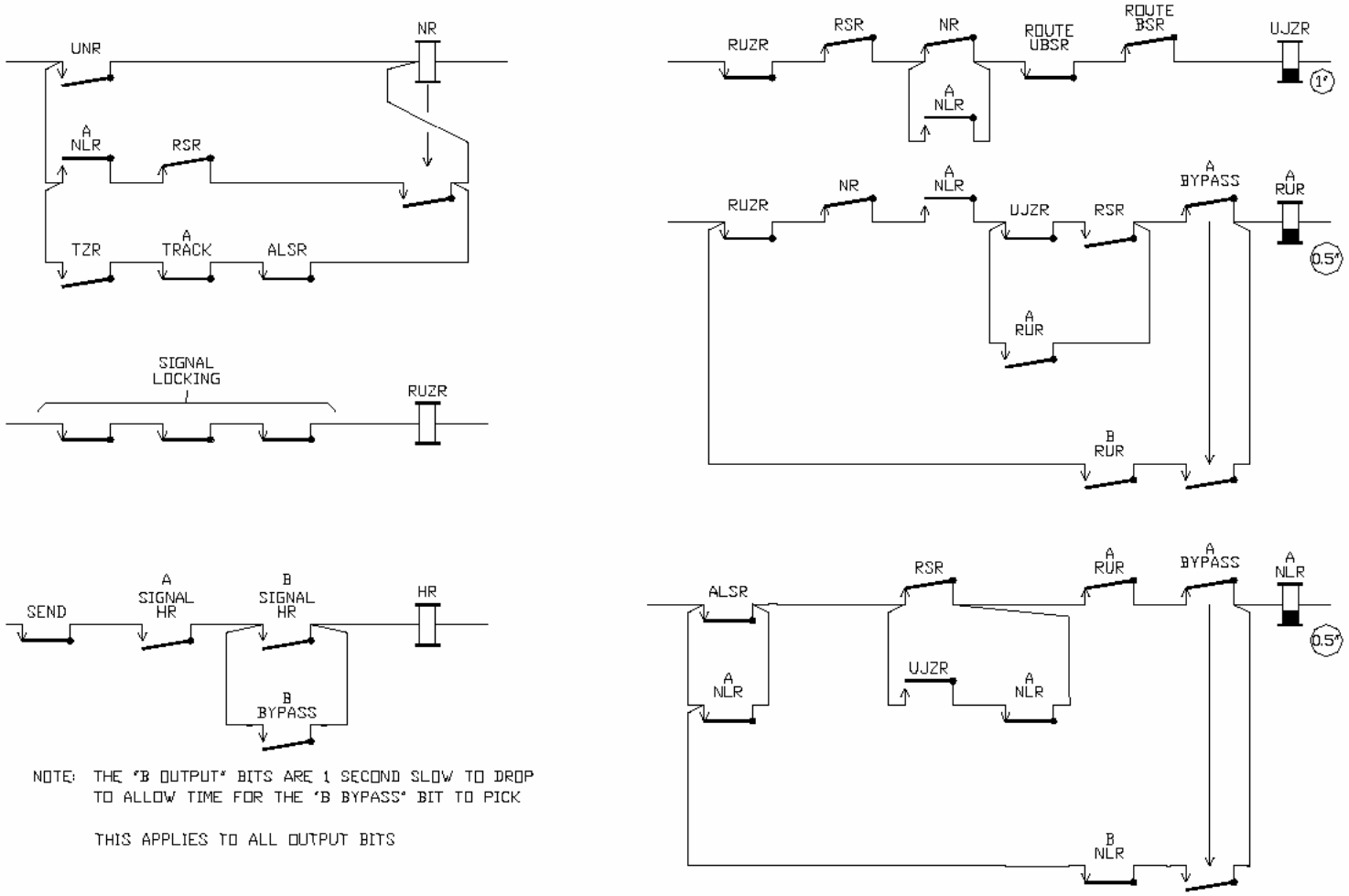
```
ASSIGN        (B_MASTER_ONLINE * ~A_MASTER_ONLINE) + ~BOOT_UP_JR_                    TO A_BYPASS;
```



SYNCHRONISATION OF SIGNALS – Superseded NX Style

NOTES:

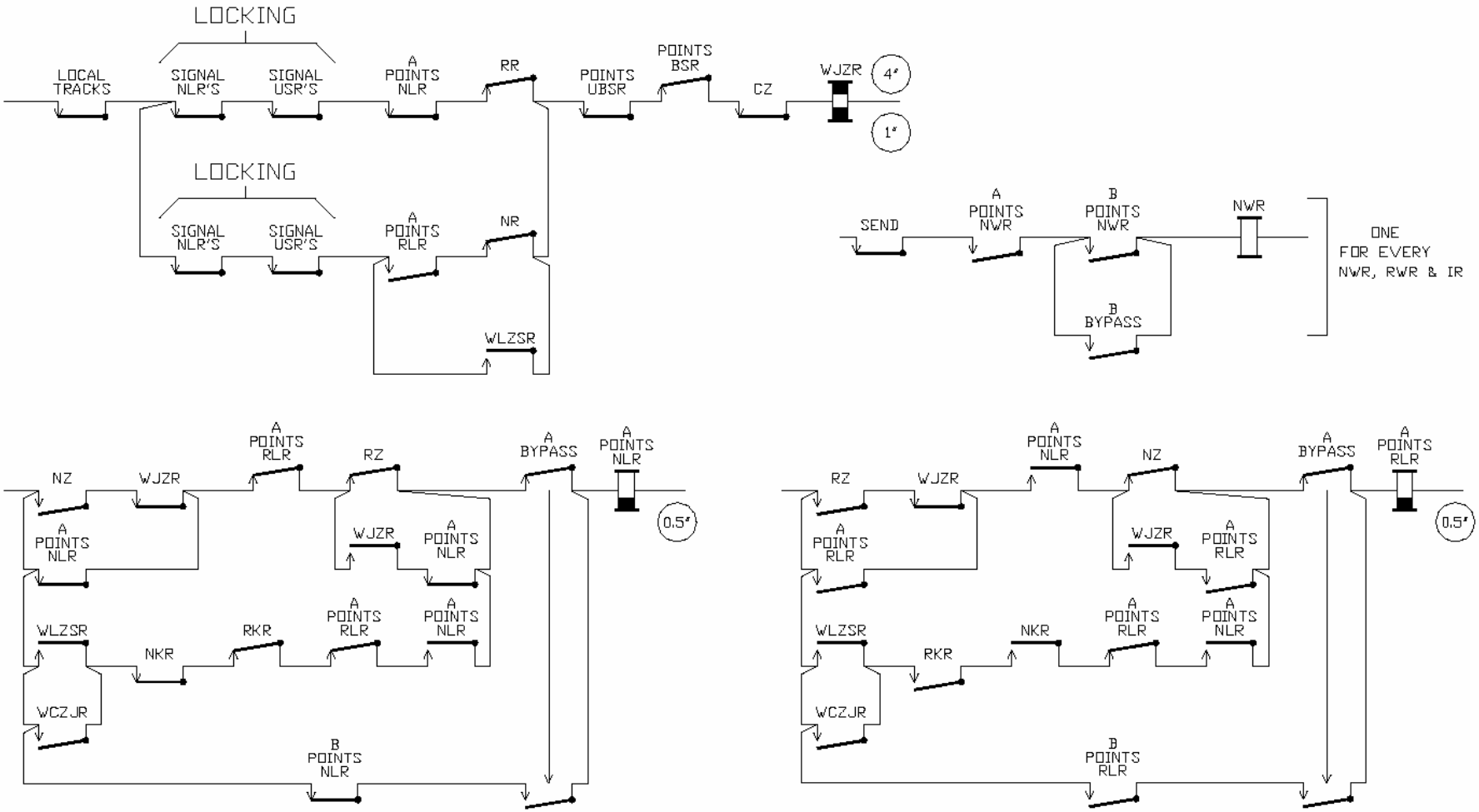
- THE "UJZR" BIT IS 1 SECOND SLOW TO DROP TO ALLOW FOR THE RUR TO PICK.
- THE SIGNAL LOCK RELAYS ARE 0.5 SECONDS SLOW TO DROP TO ALLOW FOR THE SWITCHING OF "A BYPASS".



NOTE: THE "B OUTPUT" BITS ARE 1 SECOND SLOW TO DROP TO ALLOW TIME FOR THE "B BYPASS" BIT TO PICK

THIS APPLIES TO ALL OUTPUT BITS

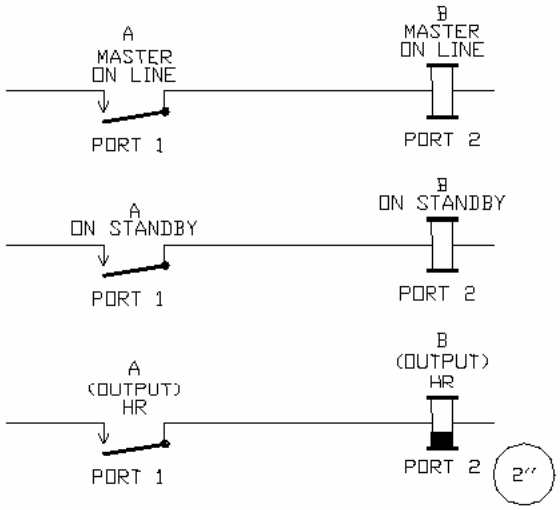
SYNCHRONISATION OF POINTS – Superseded NX Style



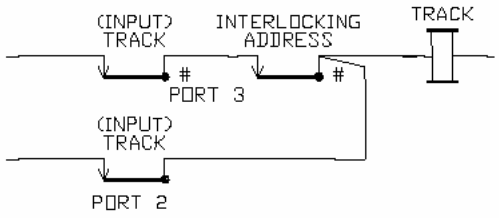
SYNCHRONISATION OF INTERLOCKING MASTERS -Superseded NX Style

NOTES:

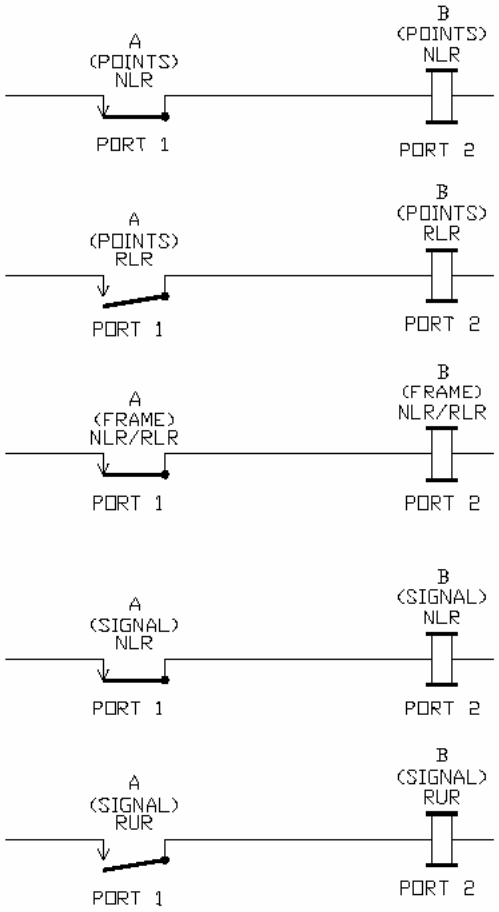
ALL INPUT BITS ARE RECEIVED FROM PORT 2.
ALL OUTPUT BITS SENT FROM PORT 1.



ALL OUTPUT BITS AT PORT 3 ARE ALSO INPUTS AT PORT 2
THESE MUST BE 2 or 2.5 SECONDS SLOW TO DROP,
PREVENTING TOO MANY BITS CHANGING STATE AT ONE TIME



APPLIES TO ALL PORT 3 INPUT BITS
(EXCLUDING ARBITRATION BITS)
THESE BITS ARE THE OUTPUTS IN PORT 1.



Attachment B – Test Scenarios

Test individual operation

Power up A side and test operation.	Starts, goes on-line and works correctly after NO_SYNC timeout.
Power down A side then power up B side and test operation.	Starts, goes on-line and works correctly.

Test hot standby operation

Power up A then B and test operation with A as master online	Including power off, on and disruption of B	No impact on outputs or indications
Power off both A and B then Power up B, then A and test operation with B as master online	Including power off, on and disruption of A	No impact on outputs or indications
Power up A then B and test operation with A as master online	Fail over from A to B and then B to A by pressing reset on the online master	No impact on outputs or indications
Power up A then B and test operation with both as master online	Fail A and restore, Fail B and restore	No impact on outputs or indications
Test controls for controlled signalling objects	Include inconsistencies and timing	
Test disruption of indications		
Test correspondences of controls and indications		

Test operation with failed hot standby link, in controlled mode

A master online fail dual link	B loses on-standby due to the other being okay, A retains on-standby and control system leaves A as master
Fail online A unit	B regains on-standby when A fails, control system requests B as master, and it goes online after NO_SYNC timeout
Reboot failed A unit	A does not get to on-standby due to the other being okay
Fail online B unit	A regains on-standby when B fails, control system requests A as master, and it goes online after NO_SYNC timeout
B master online fail dual link	A loses on-standby due to the other being okay, B retains on-standby and control system leaves B as master
Fail online B unit	A regains on-standby when B fails, control system requests A as master, and it goes online after NO_SYNC timeout.
Reboot failed B unit	B does not get to on-standby due to the other being okay
Fail online A unit	B regains on-standby when A fails, control system requests B as master, and it goes online after NO_SYNC timeout
A & B master online fail dual link	B loses on-standby due to loss of dual_master_ok, and the A being okay, A retains on-standby and control system keeps a set as master

Fail online A unit	B regains on-standby when A fails, control system requests B as master, and it goes online after NO_SYNC timeout.
Reboot failed A unit	A does not get to on-standby due to B being okay
Fail online B unit	A regains on-standby when B fails, control system requests A as master, and it goes online after NO_SYNC timeout
Power on A and wait for it to stabilise	A get on-standby after boot up timer with other not okay and control systems sets A as online and it goes online after NO_SYNC timeout.
Power on B	B does not get to on-standby
Power on B and wait for it to stabilise	B get on-standby after boot up timer and control systems sets A as online and it goes online after NO_SYNC timeout
Power on A	A does not get to on-standby
Power on A and B at the same time	If non-duplicated slaves – neither get to on-standby due to both being okay when boot up time times out. If duplicated slaves – neither get to on-standby due to both being okay when boot up timer times out (using cps.status). Both get to on-standby due to neither being online (using online status) and the control system selects one as master, which then goes online after NO_SYNC timeout. The other then loses its on-standby status.

Duplicated masters with non-duplicated slaves

Normal operation is with synchronisation and comparison of outputs.

Boot_up timer is required to delay comparison of outputs until all time release of locking (ALSJR's and TJR's) have timed out to prevent the freshly started Microlok providing more restrictive outputs.

A single system startup could bypass the boot_up timer but will it provide a significant benefit?

Operation whilst the dual link that provides synchronisation is failed will be by a cold standby arrangement.

Cold standby change over is controlled by the NO SYNCH timer.

Should this be the same time as the boot-up JR as it is to cover the same issues? Or add an amount for routes to normalise and trains to come to a stand. Assuming 1200m between signals and 20m/s average (72km/hr) which is about 60 sec or 20% longer tha n the longest ALSJR.

Starting both masters with dual link failed.

If both fail then start at the same time with the dual link failed then neither will reach on_standby.

Fully duplicated Microloks with synchronisation

Normal operation is with synchronisation and comparison of outputs.

Boot_up timer is required to delay comparison of outputs until all time release of locking (ALSJR's and TJR's) have timed out to prevent the freshly started Microlok providing more restrictive outputs.

Operation whilst the dual link that provides synchronisation is failed will be by a cold standby arrangement.

Cold standby change over is controlled by the NO SYNCH timer.

Should this be the same time as the boot-up JR as it is to cover the same issues? Or add an amount for routes to normalise and trains to come to a stand

Starting both masters with dual link failed.

If both fail then start at the same time with the dual link failed then neither will reach on_standby.

Hot Standby Single interlocking master Test Case with non-duplicated slaves

Initial conditions is: Both interlocking master Microlok card files turned off. Control System turned on. Slaves turned on

Event	Result	Status
Turn ON Interlocking Master A	Application starts and set CPS.ENABLE	Not on _standby and all outputs to slaves are OFF.
Wait		
Wait		
Wait		

BOOT_UP
A_BYPASS
B_BYPASS
SEND
A_ON_STANDBY
A_ON_LINE
B_ON_LINE
B_ON_STANDBY
DUAL_LINK_OK
ONLY_ONE_MASTER